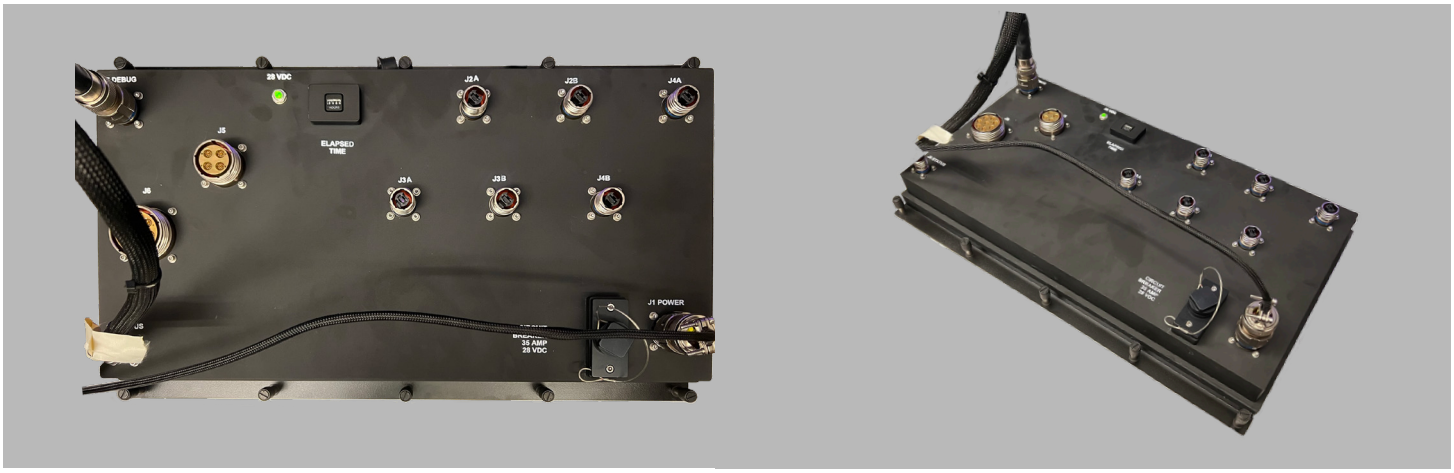
156-CHANNEL RUGGED ETHERNET SWITCH

PDS - 340



DESCRIPTION

Amphenol's Rugged 156-Channel Ethernet Switch Box is conduction cooled and configurable for system connectivity, speeds, port types, and interoperation with various high-speed media converters and connectors for system interfacing.

This switch box features 12 copper ports and 144 fiber optic ports, each capable of 1GBase-SX, 10GBase-SR, 40GBase-SR4, 25GBase-SR, and 100GBase-SR4. In Amphenol's state of the art communications testing center, the switch boxes are aggressively tested at line rates to RFC 2889 for switching and RFC 2544 for L2/L3 performance, latency, packet forwarding, and other key metrics.

The switch is manufactured using derivatives of Amphenol's MIL-DTL-38999 Series connectors. These connectors contain standard AS39029 qualified Size 22D contacts, Octonet contacts, and 48F MT Ferrule Fiber Optic contact assemblies.

Amphenol's Octonet Contacts are a proven design used in a variety of Military Programs. The Octonet is a Size 8 contact which houses (4) differential pair contacts. It is a 100 Ohm impedance contact, capable of a data rate of 4 Gbps maximum per contact pair. The contact system has been tested and passed all the Qualification Requirements of an AS39029 contact. The MT ferrules are used for fiber optic Ethernet ports and the AS39029 style contacts are used for power inputs and management functions.





Jared Sibrava • Phone: (607) 643 - 1845 • Email: jsibrava@amphenol-aao.com
amphenol-aerospace.com

12-CHANNEL 10G COPPER RUGGED ETHERNET SWITCH

FEATURES & BENEFITS

- 144 fiber optic non-blocking switched Ethernet ports capable of 1GBase-SX, 10GBase-SR, 40GBase-SR4, 25GBase-SR, and 100GBase-SR4 protocols.
- 12 channels of copper capable of 10GBase-T
- 28V MIL-STD-704A input module; VICOR MFM and DC/DC mil-spec power supply with hold-up capacitor and in-rush current limiting circuit.
- Built-in test functionality for power up, initiated, and continuous operation.
- Host management processor:
    - Multicast
    - Link Aggregation Control Protocol (LACP)
    - Protocol-Independent Multicast (PIM)
    - Internet Group Management Protocol (IGMP)
    - Simple Network Management Protocol (SNMP)
    - Capable of supporting thousands of virtual local area networks (VLAN) each with its own dynamic host configuration protocol (DHCP) server for various devices within the VLAN
    - Configurable cross VLAN multicast routing
    - Storm-prevention
    - IPV4 and IPV6 support
    - Spanning tree protocol
    - Temperature and current monitoring and thermal shutdown in the event of over temperature
    - SSH, NTP, PTP, TFTP, secure FTP support
    - Custom configuration files
    - Web server interaction
    - Other

    - Link status on demand, port counter status, configurable port speed/routing, ARP list, drop report, ping, MTU configuration, LUA configuration
- Power connector, debug connector, maintenance connector – all D38999's
- Mil-Spec black painted chassis with cold plate external conduction cooling

ENVIRONMENTAL

- -55 C to 85 C operating depending on altitude – perfect for military aerospace environments
- Conduction cooled for cold plate interface
- Shock, vibration, bench handling, EMI/EMC per 461E, 704F power, salt/fog/dust, fluids/rain, explosive atmosphere, humidity
- Plating & paint is configurable but currently Mil-Spec black paint with back cover chromated for grounding

Jared Sibrava • Phone: (607) 643 - 1845 • Email: jsibrava@amphenol-aao.com
amphenol-aerospace.com

I/O CHARTS:

I/O CHART			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J1 (POWER) 15-4P KEYING "N"	A	IN	28VDC_IN
	B	OUT	28VDC_RTN
	C	--	SAFETY GROUND / CHASSIS
	D	--	NOT CONNECTED
	SHELL	--	CHASSIS
J7 (DEBUG) 13-35P KEYING "N"	1	OUT	RS232_CONSOLE_TX
	2	IN	RS232_CONSOLE_RX
	3	--	RS232_CONSOLE_GND
	4	BI	PIC_A_PGM_PGC
	5	BI	PIC_A_PGM_PGD
	6	IN	PIC_A_PGM_3.3V
	7	OUT	PIC_A_PGM_GND
	8	BI	DEBUG_I2C_SCL
	9	BI	DEBUG_I2C_SDA
	10	BI	PIC_A_PGM_MCLR
	11	--	PIC-RS232-GND
	12	OUT	PIC-RS232-TXD
	13	IN	PIC-RS232-RXD
	14	BI	DEBUG_CPU_1GBase-T_DA+
	15		DEBUG_CPU_1GBase-T_DA-
	16		DEBUG_CPU_1GBase-T_DB+
	17		DEBUG_CPU_1GBase-T_DB-
	18		DEBUG_CPU_1GBase-T_DC+
	19		DEBUG_CPU_1GBase-T_DC-
	20		DEBUG_CPU_1GBase-T_DD+
	21		DEBUG_CPU_1GBase-T_DD-
	22	--	NOT CONNECTED
	SHELL	--	CHASSIS
J8 (STATUS/RESET) 9-35P KEYING "N"	1	IN	SWITCHBOX_RESET
	2	OUT	POWERSUPPLY_STATUS
	3	OUT	CHASSIS_STATUS
	4	OUT	TEMPERATURE_WARNING_STATUS
	5	--	RESET_RTN
	6	--	NOT CONNECTED
	SHELL	--	CHASSIS

I/O CHARTS:

I/O CHART

CONNECTOR DESCRIPTION	PIN NO	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO
J5 19-ABS 4X OCTO KEYING "N"	B1	BI	10GBase-T_DA+	145
	B2	BI	10GBase-T_DA-	
	B3	BI	10GBase-T_DB+	
	B4	BI	10GBase-T_DB-	
	B5	BI	10GBase-T_DC+	
	B6	BI	10GBase-T_DC-	
	B7	BI	10GBase-T_DD+	
	B8	BI	10GBase-T_DD-	
	F1	BI	10GBase-T_DA+	146
	F2	BI	10GBase-T_DA-	
	F3	BI	10GBase-T_DB+	
	F4	BI	10GBase-T_DB-	
	F5	BI	10GBase-T_DC+	
	F6	BI	10GBase-T_DC-	
	F7	BI	10GBase-T_DD+	
	F8	BI	10GBase-T_DD-	
	K1	BI	10GBase-T_DA+	147
	K2	BI	10GBase-T_DA-	
	K3	BI	10GBase-T_DB+	
	K4	BI	10GBase-T_DB-	
	K5	BI	10GBase-T_DC+	
	K6	BI	10GBase-T_DC-	
	K7	BI	10GBase-T_DD+	
	K8	BI	10GBase-T_DD-	
	P1	BI	10GBase-T_DA+	148
	P2	BI	10GBase-T_DA-	
	P3	BI	10GBase-T_DB+	
	P4	BI	10GBase-T_DB-	
	P5	BI	10GBase-T_DC+	
	P6	BI	10GBase-T_DC-	
	P7	BI	10GBase-T_DD+	
	P8	BI	10GBase-T_DD-	
	B-OUTER	--	CHASSIS	--
	F-OUTER	--	CHASSIS	--
	K-OUTER	--	CHASSIS	--
	P-OUTER	--	CHASSIS	--
	SHELL	--	CHASSIS	--

CONNECTOR DESCRIPTION	PIN NO	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO
J6 25-8S 8X OCTO KEYING "N"	A1	BI	10GBase-T_DA+	149
	A2	BI	10GBase-T_DA-	
	A3	BI	10GBase-T_DB+	
	A4	BI	10GBase-T_DB-	
	A5	BI	10GBase-T_DC+	
	A6	BI	10GBase-T_DC-	
	A7	BI	10GBase-T_DD+	
	A8	BI	10GBase-T_DD-	
	B1	BI	10GBase-T_DA+	150
	B2	BI	10GBase-T_DA-	
	B3	BI	10GBase-T_DB+	
	B4	BI	10GBase-T_DB-	
	B5	BI	10GBase-T_DC+	
	B6	BI	10GBase-T_DC-	
	B7	BI	10GBase-T_DD+	
	B8	BI	10GBase-T_DD-	
	C1	BI	10GBase-T_DA+	151
	C2	BI	10GBase-T_DA-	
	C3	BI	10GBase-T_DB+	
	C4	BI	10GBase-T_DB-	
	C5	BI	10GBase-T_DC+	
	C6	BI	10GBase-T_DC-	
	C7	BI	10GBase-T_DD+	
	C8	BI	10GBase-T_DD-	
	D1	BI	10GBase-T_DA+	152
	D2	BI	10GBase-T_DA-	
	D3	BI	10GBase-T_DB+	
	D4	BI	10GBase-T_DB-	
	D5	BI	10GBase-T_DC+	
	D6	BI	10GBase-T_DC-	
	D7	BI	10GBase-T_DD+	
	D8	BI	10GBase-T_DD-	
	A-OUTER	--	CHASSIS	--
	B-OUTER	--	CHASSIS	--
	C-OUTER	--	CHASSIS	--
	D-OUTER	--	CHASSIS	--
	SHELL	--	CHASSIS	--

CONNECTOR DESCRIPTION	PIN NO	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO
J6 25-8S 8X OCTO KEYING "N"	E1	BI	10GBase-T_DA+	153
	E2	BI	10GBase-T_DA-	
	E3	BI	10GBase-T_DB+	
	E4	BI	10GBase-T_DB-	
	E5	BI	10GBase-T_DC+	
	E6	BI	10GBase-T_DC-	
	E7	BI	10GBase-T_DD+	
	E8	BI	10GBase-T_DD-	
	F1	BI	10GBase-T_DA+	154
	F2	BI	10GBase-T_DA-	
	F3	BI	10GBase-T_DB+	
	F4	BI	10GBase-T_DB-	
	F5	BI	10GBase-T_DC+	
	F6	BI	10GBase-T_DC-	
	F7	BI	10GBase-T_DD+	
	F8	BI	10GBase-T_DD-	
	G1	BI	10GBase-T_DA+	155
	G2	BI	10GBase-T_DA-	
	G3	BI	10GBase-T_DB+	
	G4	BI	10GBase-T_DB-	
	G5	BI	10GBase-T_DC+	
	G6	BI	10GBase-T_DC-	
	G7	BI	10GBase-T_DD+	
	G8	BI	10GBase-T_DD-	
	H1	BI	10GBase-T_DA+	156
	H2	BI	10GBase-T_DA-	
	H3	BI	10GBase-T_DB+	
	H4	BI	10GBase-T_DB-	
	H5	BI	10GBase-T_DC+	
	H6	BI	10GBase-T_DC-	
	H7	BI	10GBase-T_DD+	
	H8	BI	10GBase-T_DD-	
	E-OUTER	--	CHASSIS	--
	F-OUTER	--	CHASSIS	--
	G-OUTER	--	CHASSIS	--
	H-OUTER	--	CHASSIS	--
	SHELL	--	CHASSIS	--

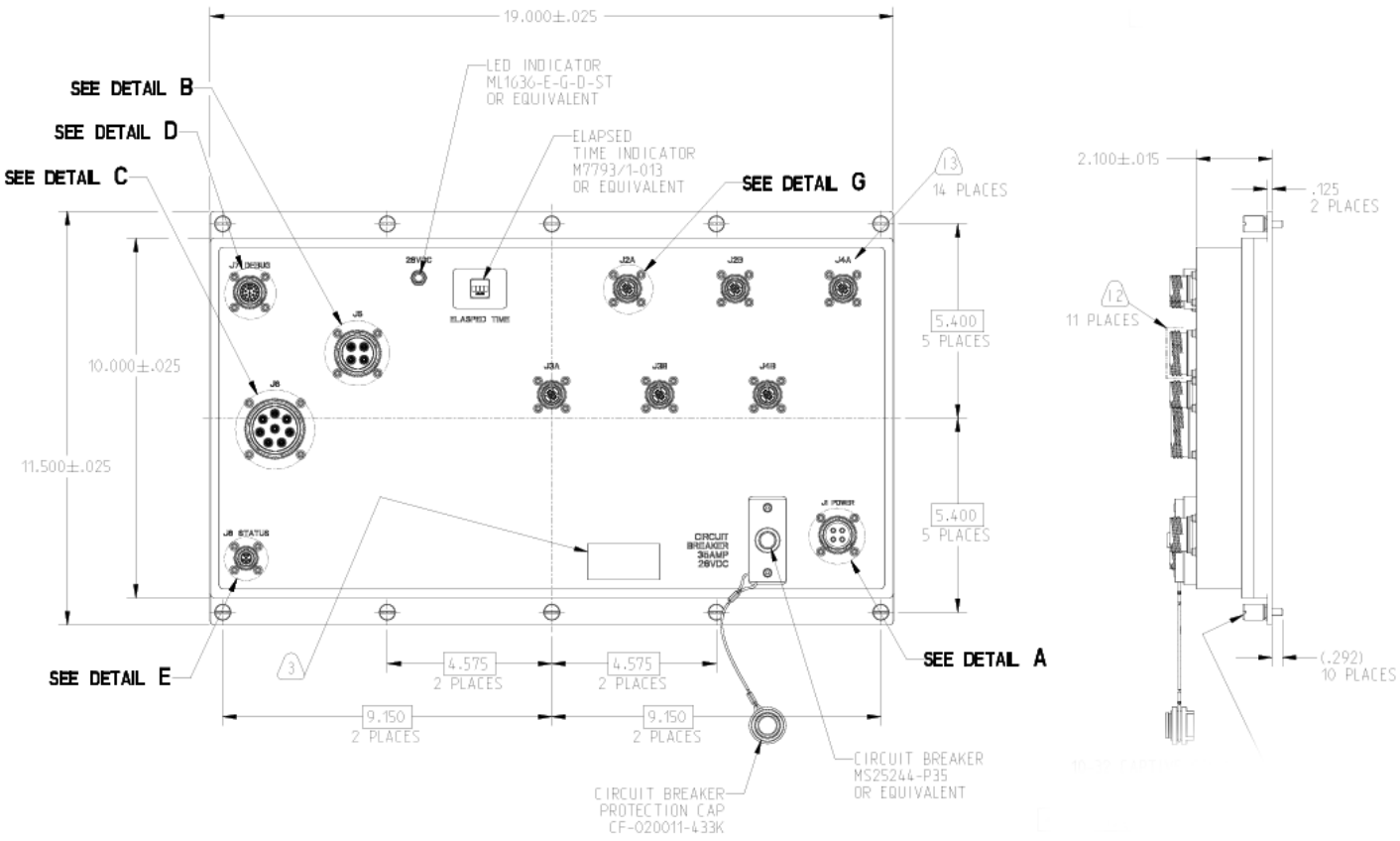
I/O CHART

CONNECTOR DESCRIPTION	PIN NO	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO
J2A 11-01S 1X 48F MT KEYING "N"	1	IN	25GBase-SR_RX	12
	2	IN	25GBase-SR_RX	11
	3	IN	25GBase-SR_RX	10
	4	IN	25GBase-SR_RX	9
	5	IN	25GBase-SR_RX	8
	6	IN	25GBase-SR_RX	7
	7	IN	25GBase-SR_RX	6
	8	IN	25GBase-SR_RX	5
	9	IN	25GBase-SR_RX	4
	10	IN	25GBase-SR_RX	3
	11	IN	25GBase-SR_RX	2
	12	IN	25GBase-SR_RX	1
	13	OUT	25GBase-SR_TX	12
	14	OUT	25GBase-SR_TX	11
	15	OUT	25GBase-SR_TX	10
	16	OUT	25GBase-SR_TX	9
	17	OUT	25GBase-SR_TX	8
	18	OUT	25GBase-SR_TX	7
	19	OUT	25GBase-SR_TX	6
	20	OUT	25GBase-SR_TX	5
	21	OUT	25GBase-SR_TX	4
	22	OUT	25GBase-SR_TX	3
	23	OUT	25GBase-SR_TX	2
	24	OUT	25GBase-SR_TX	1
	25	IN	25GBase-SR_RX	24
	26	IN	25GBase-SR_RX	23
	27	IN	25GBase-SR_RX	22
	28	IN	25GBase-SR_RX	21
	29	IN	25GBase-SR_RX	20
	30	IN	25GBase-SR_RX	19
	31	IN	25GBase-SR_RX	18
	32	IN	25GBase-SR_RX	17
	33	IN	25GBase-SR_RX	16
	34	IN	25GBase-SR_RX	15
	35	IN	25GBase-SR_RX	14
	36	IN	25GBase-SR_RX	13
	37	OUT	25GBase-SR_TX	24
	38	OUT	25GBase-SR_TX	23
	39	OUT	25GBase-SR_TX	22
	40	OUT	25GBase-SR_TX	21
	41	OUT	25GBase-SR_TX	20
	42	OUT	25GBase-SR_TX	19
	43	OUT	25GBase-SR_TX	18
	44	OUT	25GBase-SR_TX	17
	45	OUT	25GBase-SR_TX	16
	46	OUT	25GBase-SR_TX	15
	47	OUT	25GBase-SR_TX	14
	48	OUT	25GBase-SR_TX	13

CONNECTOR DESCRIPTION	PIN NO	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO
J2B 11-01S 1X 48F MT KEYING "A"	1	IN	25GBase-SR_RX	36
	2	IN	25GBase-SR_RX	35
	3	IN	25GBase-SR_RX	34
	4	IN	25GBase-SR_RX	33
	5	IN	25GBase-SR_RX	32
	6	IN	25GBase-SR_RX	31
	7	IN	25GBase-SR_RX	30
	8	IN	25GBase-SR_RX	29
	9	IN	25GBase-SR_RX	28
	10	IN	25GBase-SR_RX	27
	11	IN	25GBase-SR_RX	26
	12	IN	25GBase-SR_RX	25
	13	OUT	25GBase-SR_TX	36
	14	OUT	25GBase-SR_TX	35
	15	OUT	25GBase-SR_TX	34
	16	OUT	25GBase-SR_TX	33
	17	OUT	25GBase-SR_TX	32
	18	OUT	25GBase-SR_TX	31
	19	OUT	25GBase-SR_TX	30
	20	OUT	25GBase-SR_TX	29
	21	OUT	25GBase-SR_TX	28
	22	OUT	25GBase-SR_TX	27
	23	OUT	25GBase-SR_TX	26
	24	OUT	25GBase-SR_TX	25
	25	IN	25GBase-SR_RX	48
	26	IN	25GBase-SR_RX	47
	27	IN	25GBase-SR_RX	46
	28	IN	25GBase-SR_RX	45
	29	IN	25GBase-SR_RX	44
	30	IN	25GBase-SR_RX	43
	31	IN	25GBase-SR_RX	42
	32	IN	25GBase-SR_RX	41
	33	IN	25GBase-SR_RX	40
	34	IN	25GBase-SR_RX	39
	35	IN	25GBase-SR_RX	38
	36	IN	25GBase-SR_RX	37
	37	OUT	25GBase-SR_TX	48
	38	OUT	25GBase-SR_TX	47
	39	OUT	25GBase-SR_TX	46
	40	OUT	25GBase-SR_TX	45
	41	OUT	25GBase-SR_TX	44
	42	OUT	25GBase-SR_TX	43
	43	OUT	25GBase-SR_TX	42
	44	OUT	25GBase-SR_TX	41
	45	OUT	25GBase-SR_TX	40
	46	OUT	25GBase-SR_TX	39
	47	OUT	25GBase-SR_TX	38
	48	OUT	25GBase-SR_TX	37

CONNECTOR DESCRIPTION	PIN NO	DATA DIRECTION	SIGNAL NAME	ETHERNET PORT NO
J3A 11-01S 1X 48F MT KEYING "B"	1	IN	25GBase-SR_RX	60
	2	IN	25GBase-SR_RX	59
	3	IN	25GBase-SR_RX	58
	4	IN	25GBase-SR_RX	57
	5	IN	25GBase-SR_RX	56
	6	IN	25GBase-SR_RX	55
	7	IN	25GBase-SR_RX	54
	8	IN	25GBase-SR_RX	53
	9	IN	25GBase-SR_RX	52
	10	IN	25GBase-SR_RX	51
	11	IN	25GBase-SR_RX	50
	12	IN	25GBase-SR_RX	49
	13	OUT	25GBase-SR_TX	60
	14	OUT	25GBase-SR_TX	59
	15	OUT	25GBase-SR_TX	58
	16	OUT	25GBase-SR_TX	57
	17	OUT	25GBase-SR_TX	56
	18	OUT	25GBase-SR_TX	55
	19	OUT	25GBase-SR_TX	54
	20	OUT	25GBase-SR_TX	53
	21	OUT	25GBase-SR_TX	52
	22	OUT	25GBase-SR_TX	51
	23	OUT	25GBase-SR_TX	50
	24	OUT	25GBase-SR_TX	49
	25	IN	25GBase-SR_RX	72
	26	IN	25GBase-SR_RX	71
	27	IN	25GBase-SR_RX	70
	28	IN	25GBase-SR_RX	69
	29	IN	25GBase-SR_RX	68
	30	IN	25GBase-SR_RX	67
	31	IN	25GBase-SR_RX	66
	32	IN	25GBase-SR_RX	65
	33	IN	25GBase-SR_RX	64
	34	IN	25GBase-SR_RX	63
	35	IN	25GBase-SR_RX	62
	36	IN	25GBase-SR_RX	61
	37	OUT	25GBase-SR_TX	72
	38	OUT	25GBase-SR_TX	71
	39	OUT	25GBase-SR_TX	70
	40	OUT	25GBase-SR_TX	69
	41	OUT	25GBase-SR_TX	68
	42	OUT	25GBase-SR_TX	67
	43	OUT	25GBase-SR_TX	66
	44	OUT	25GBase-SR_TX	65
	45	OUT	25GBase-SR_TX	64
	46	OUT	25GBase-SR_TX	63
	47	OUT	25GBase-SR_TX	62
	48	OUT	25GBase-SR_TX	61

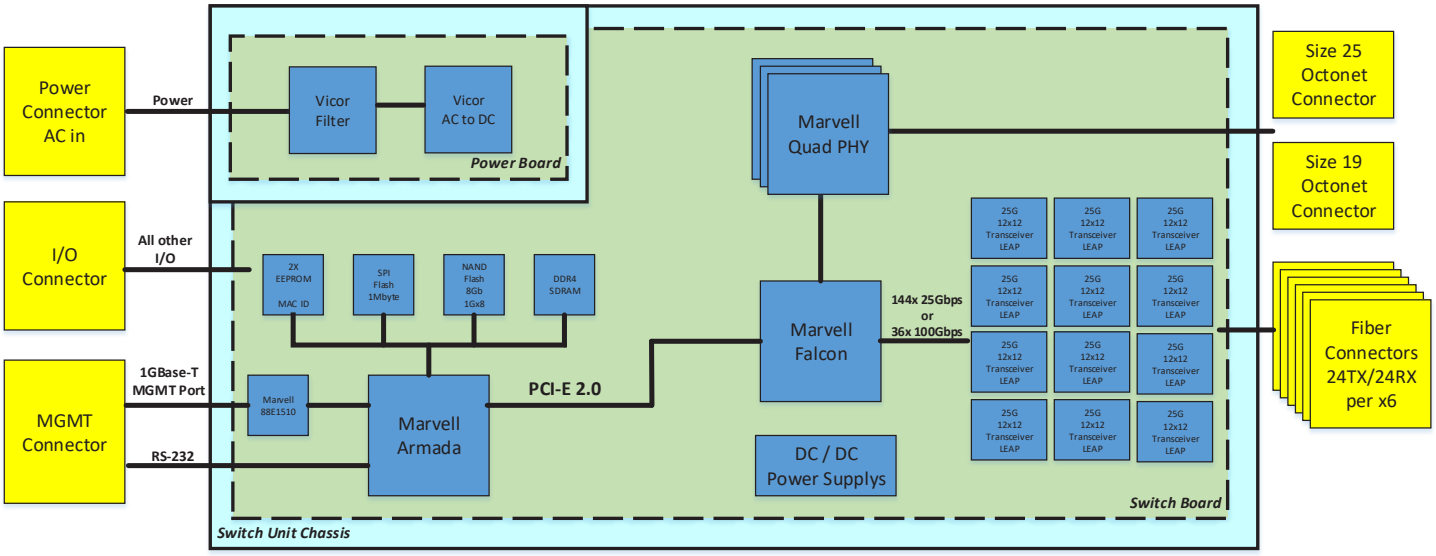
DIMENSIONAL DRAWING:



Jared Sibrava • Phone: (607) 643 - 1845 • Email: jsibrava@amphenol-aao.com
amphenol-aerospace.com

12-CHANNEL 10G COPPER RUGGED ETHERNET SWITCH

BLOCK DIAGRAM



ORDERING INFORMATION	
CF-020400-077	156 CHANNEL ETHERNET SWITCH

Jared Sibrava • Phone: (607) 643 - 1845 • Email: jsibrava@amphenol-aao.com
amphenol-aerospace.com

SOFTWARE FEATURES

Stacking
Stacking Ring Topology
Stacking Chain Topology
Stacking Members and Unit ID
Removing and Replacing Stacking Members
Exchanging Stacking Members
Switching the Stacking Master
Configuring System Time
Configuring Daylight Savings Time
Configuring SNTP
Polling for Unicast Time Information
Polling for Anycast Time Information
Broadcast Time Information
Defining SNTP Settings
Configuring Device Security
Configuring Management Security
Configuring Authentication Methods
Defining Access Profiles
Defining Profile Rules
Defining Authentication Profiles
Mapping Authentication Methods
Defining RADIUS Settings
Defining TACACS+ Authentication
Configuring Passwords
Defining Local Users
Defining Line Passwords
Defining Enable Passwords
Configuring Network Security
Network Security Overview
Port-Based Authentication
Advanced Port-Based Authentication
Defining Port Authentication Properties
Defining Port Authentication
Configuring Multiple Hosts
Defining Authentication Hosts
Viewing EAP Statistics
Defining Access Control Lists
Defining IP Based Access Control Lists
Defining MAC Based Access Control Lists
Binding Device Security ACLs
Managing Port Security
Enabling Storm Control
Configuring System Logs
Defining General Log Properties
Viewing Memory Logs
Viewing Flash Logs
Configuring Interfaces
Configuring Ports
Aggregating Ports
Configuring LACP
Configuring VLANs
Defining VLAN Properties
Defining VLAN Membership
Defining VLAN Interface Settings
Configuring GARP
Defining GARP
Defining GVRP
Viewing GVRP Statistics

Defining IP Addresses
Configuring IP Addressing
Defining IP Addresses
Defining ARP
Defining Domain Name Servers
Defining DNS Servers
Defining DNS Host Mapping
Defining the Forwarding Database
Defining Static Forwarding Database Entries
Defining Dynamic Forwarding Database Entries
Configuring Spanning Tree
Defining Classic Spanning Tree
Defining STP on Interfaces
Defining Rapid Spanning Tree
Defining Multiple Spanning Tree
Defining MSTP Instance Settings
Defining MSTP Interface Settings
Configuring SNMP
SNMP v1 and v2c
SNMP v3
Configuring SNMP Security
Defining SNMP Security
Defining SNMP View
Defining SNMP Group Profiles
Defining SNMP Group Members
Defining SNMP Communities
SNMP Communities Basic Table
SNMP Communities Advanced Table
Configuring SNMP Notifications
Defining SNMP Notification Global Parameters .
Defining SNMP Notification Filters
Defining SNMP Notification Recipients
SNMPv1,2c Notification Recipients
SNMPv3 Notification Recipients
Configuring Multicast Forwarding
Multicast Forwarding
Typical Multicast Setup
Multicast Operation
Multicast Registration
Multicast Address Properties
Defining Multicast Properties
Adding MAC Group Address
Adding IP Multicast Groups
Configuring IGMP Snooping
Configuring MLD Snooping
Viewing IGMP/MLD IP Multicast Groups
Defining Multicast Router Ports
Defining Forward All Multicast
Defining Unregistered Multicast Settings

Managing System Files
Downloading System Files
Firmware Download
Configuration Download
Uploading System Files
Upload Type
Software Image Upload
Configuration Upload
Copying Files
Restoring the Default Configuration File
Configuring Quality of Service
Quality of Service Overview
VPT Classification Information
CoS Services
Defining General QoS Settings
Configuring QoS General Settings
Restoring Factory Default QoS Interface Settings
Defining Queues
Defining Bandwidth Settings
Mapping CoS Values to Queues
Mapping DSCP Values to Queues
Defining QoS Basic Mode
Defining Basic Mode Settings
Rewriting Basic Mode DSCP Values
Defining QoS Advanced Mode
Setting Policy Binding
Managing Device Diagnostics
Configuring Port Mirroring
Viewing Statistics
Viewing Interface Statistics
Viewing Interface Statistics
Receive Statistics
Transmit Statistics
Viewing Etherlike Statistics
Managing RMON Statistics
Viewing RMON Statistics
Configuring RMON History
Defining RMON History Control
Viewing the RMON History Table
Configuring RMON Events
Defining RMON Events Control
Viewing the RMON Events Logs
Defining RMON Alarms