6U VPX SOSA ALIGNED VITA 91 ETHERNET SWITCH

Amphenol MILITARY HIGH SPEED

Ruggedized High Density Ethernet switch with 25G or 50G Fiber

PDS - 372



SOSA V91 with 50G Fiber



SOSA V91 with 25G Fiber

DESCRIPTION

The 6U VPX V91 SOSA-aligned high-speed, high-density 25G/50 G Ethernet switches, builds on our trusted 10Gbps technology available in both 3U and 6U configurations. The 6U V91 switches are offered in two versatile configurations: 240 channels: Backplane – 192 channels at 50G; Front Panel – 48 channels at 25G; 216 channels: Backplane – 192 channels at 50G; Front Panel – 24 channels at 50G. Designed with flexibility in mind, these switches are fully configurable to meet diverse system requirements. They provide adaptability in system connectivity, speeds, port types, and seamless interoperability with various media converters and connectors. This unmatched versatility stems from cutting-edge product design and engineering innovation. To optimize usability, the switches feature advanced management software that includes a command-line interface (CLI), SNMP support, and web-based configuration tools. The software is equipped with a comprehensive suite of capabilities, including virtualization, quality of service (QoS), security, tunneling, Precision Time Protocol (PTP), and more.

FEATURES & BENEFITS

- Version 1: 240 channels: CF-02W600-10X
  - Backplane: 184 channels at 50G
  - Front Panel: 48 channels at 25G
- Version 2: 216 channels: CF-02W600-11X
  - Backplane: 184 channels at 50G
  - Front Panel: 24 channels at 50G
- Total switching throughput of 10.4 Tbps
- Line rate forward of X & Y
- L2 / L3 managed switch
- PTP IEEE 1588v1/v2 support; other specialized functions
- Available in conduction and air-cooled configurations for -40-85C environments as well as harsh vibration profiles

ORDERING INFORMATION

Part Number	Channels	Backplane	Front Panel
CF-02W600-10X	232	184@50G	48@25G
CF-02W600-11X	208	184@50G	24@50G

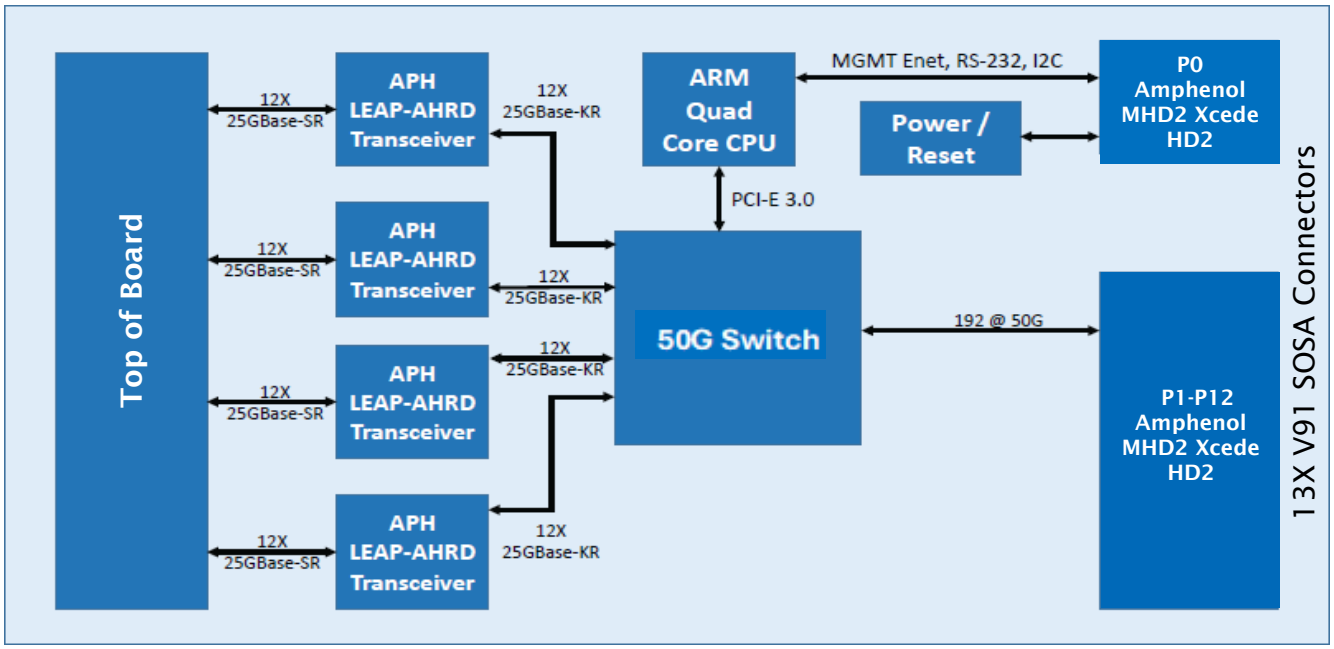
For other options, please contact the factory.

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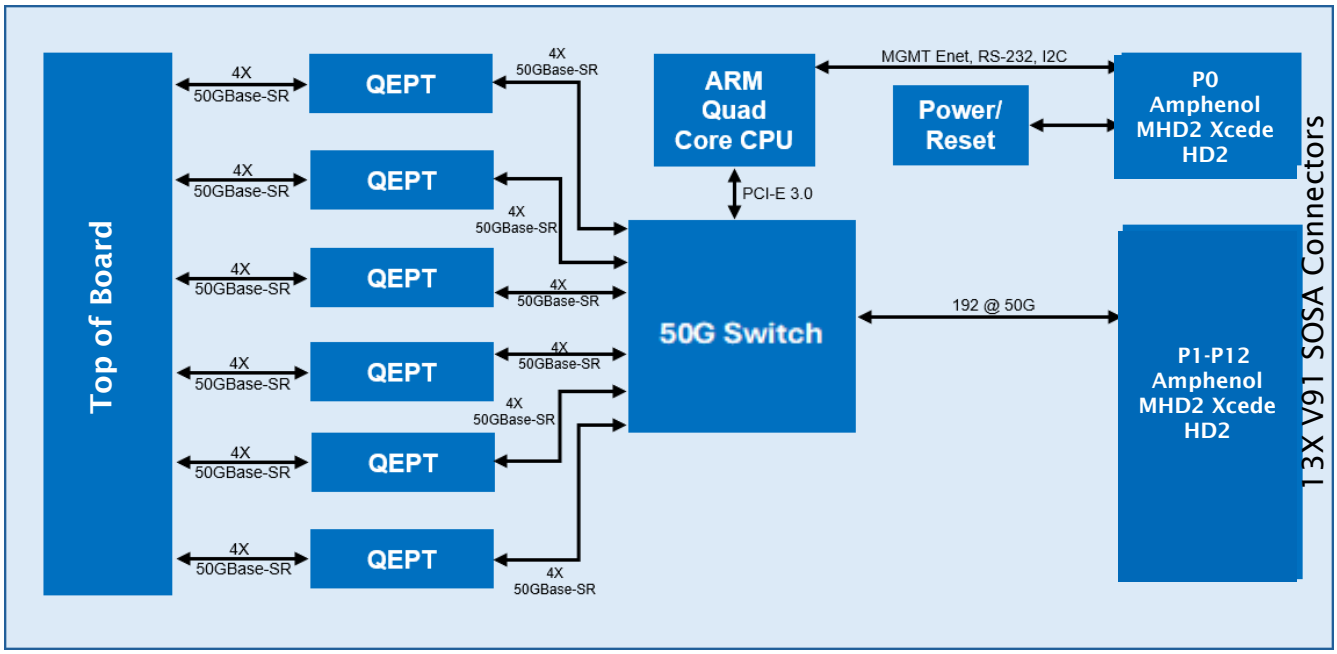
BLOCK DIAGRAMS

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CF-02W600-10X



CF-02W600-11X



ETHERNET INTERFACES

- 1X 100/1GBase-T Management Interface + RS232 Serial Console
- Version 1: 232 channels: CF-02W600-10X
  - Backplane: 184 channels at 50G
  - Front Panel: 48 channels at 25G
- Version 2: 208 channels: CF-02W600-11X
  - Backplane: 184 channels at 50G
  - Front Panel: 24 channels at 50G

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SOFTWARE FEATURES

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- **Stacking**
- Stacking Ring Topology
- Stacking Chain Topology
- Stacking Members and Unit ID
- Removing and Replacing Stacking Members
- Exchanging Stacking Members
- Switching the Stacking Master
- **Configuring System Time**
- Configuring Daylight Savings Time
- Configuring SNTP
- Polling for Unicast Time Information
- Polling for Anycast Time Information
- Broadcast Time Information
- Defining SNTP Settings
- **Configuring Device Security**
- Configuring Management Security
- Configuring Authentication Methods
- Defining Access Profiles
- Defining Profile Rules
- Defining Authentication Profiles
- Mapping Authentication Methods
- Defining RADIUS Settings
- Defining TACACS+ Authentication
- Configuring Passwords
- Defining Local Users
- Defining Line Passwords
- Defining Enable Passwords
- Configuring Network Security
- Network Security Overview
- Port-Based Authentication
- Advanced Port-Based Authentication
- Defining Port Authentication Properties
- Defining Port Authentication
- Configuring Multiple Hosts
- Defining Authentication Hosts
- Viewing EAP Statistics
- Defining Access Control Lists
- Defining IP Based Access Control Lists
- Defining MAC Based Access Control Lists
- Binding Device Security ACLs
- Managing Port Security
- Enabling Storm Control
- **Configuring System Logs**
- Defining General Log Properties
- Viewing Memory Logs
- Viewing Flash Logs
- Defining System Log Servers
- **Configuring Interfaces**
- Configuring Ports
- Aggregating Ports
- Configuring LACP

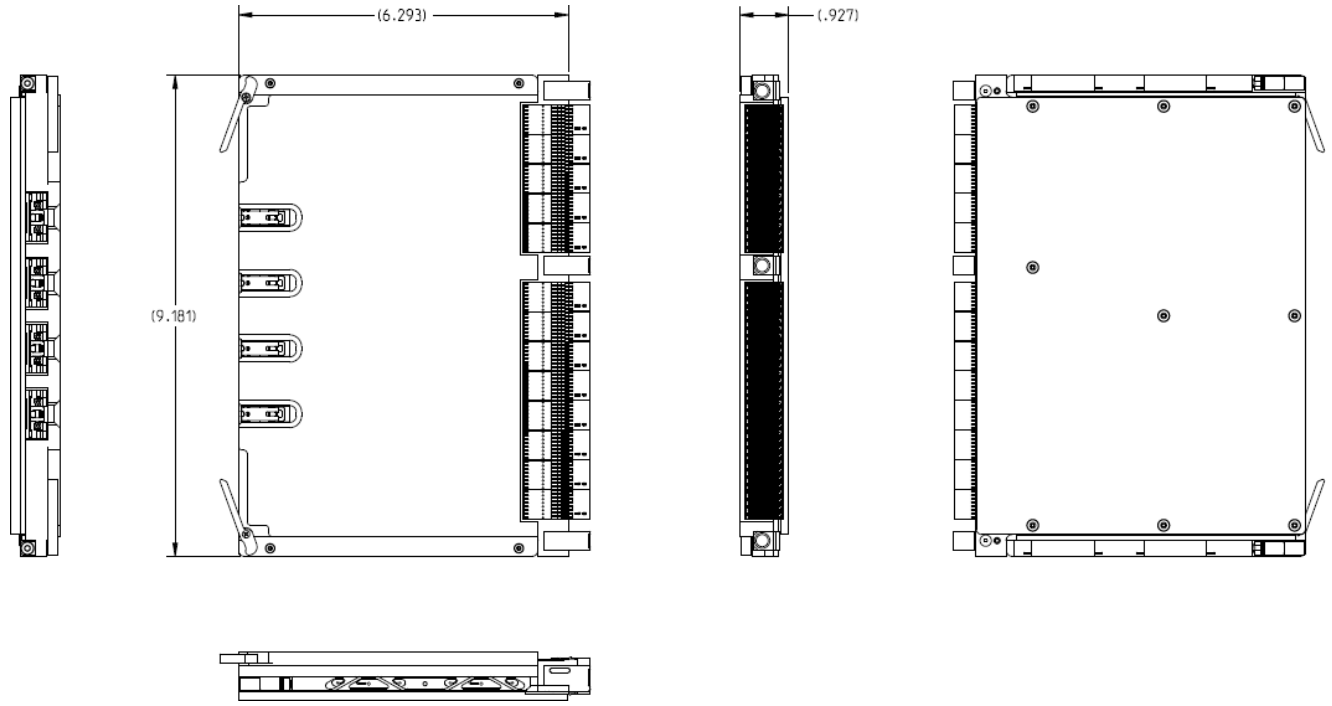
- Configuring VLANs
- Defining VLAN Properties
- Defining VLAN Membership
- Defining VLAN Interface Settings
- Configuring GARP
- Defining GARP
- Defining GVRP
- Viewing GVRP Statistics
- **Defining IP Addresses**
- Configuring IP Addressing
- Defining IP Addresses
- Defining ARP
- Defining Domain Name Servers
- Defining DNS Servers
- Defining DNS Host Mapping
- **Defining the Forwarding Database**
- Defining the Forwarding Database
- Defining Access Profiles
- **Configuring Spanning Tree**
- Defining Classic Spanning Tree
- Defining STP on Interfaces
- Defining Rapid Spanning Tree
- Defining Multiple Spanning Tree
- Defining MSTP Instance Settings
- Defining MSTP Interface Settings
- **Configuring SNMP**
- SNMP v1 and v2c
- SNMP v3
- Configuring SNMP Security
- Defining SNMP Security
- Defining SNMP View
- Defining SNMP Group Profiles
- Defining SNMP Group Members
- Defining SNMP Communities
- SNMP Communities Basic Table
- SNMP Communities Advanced Table
- Configuring SNMP Notifications
- Defining SNMP Notification Global Parameters
- Defining SNMP Notification Filters
- Defining SNMP Notification Recipients
- SNMPv1,2c Notification Recipients
- SNMPv3 Notification Recipients
- **Configuring Multicast Forwarding**
- Multicast Forwarding
- Typical Multicast Setup
- Multicast Operation
- Multicast Registration
- Multicast Address Properties
- Defining Multicast Properties
- Adding MAC Group Address
- Adding IP Multicast Groups

- Configuring IGMP Snooping
- Configuring MLD Snooping
- Viewing IGMP/MLD IP Multicast Groups
- Defining Multicast Router Ports
- Defining Forward All Multicast
- Defining Unregistered Multicast Settings
- **Managing System Files**
- Downloading System Files
- Firmware Download
- Configuration Download
- Uploading System Files
- Upload Type
- Software Image Upload
- Configuration Upload
- Copying Files
- Restoring the Default Configuration File
- **Configuring Quality of Service**
- Quality of Service Overview
- VPT Classification Information
- CoS Services
- Defining General QoS Settings
- Configuring QoS General Settings
- Restoring Factory Default QoS Interface Settings
- Defining Queues
- Defining Bandwidth Settings
- Mapping CoS Values to Queues
- Mapping DSCP Values to Queues
- Defining QoS Basic Mode
- Defining Basic Mode Settings
- Rewriting Basic Mode DSCP Values
- Defining QoS Advanced Mode
- Setting Policy Binding
- **Managing Device Diagnostics**
- Configuring Port Mirroring
- **Viewing Statistics**
- Viewing Interface Statistics
- Viewing Interface Statistics
- Receive Statistics
- Transmit Statistics
- Viewing Etherlike Statistics
- Managing RMON Statistics
- Viewing RMON Statistics
- Configuring RMON History
- Defining RMON History Control
- Viewing the RMON History Table
- Configuring RMON Events
- Defining RMON Events Control
- Viewing the RMON Events Logs
- Defining RMON Alarms

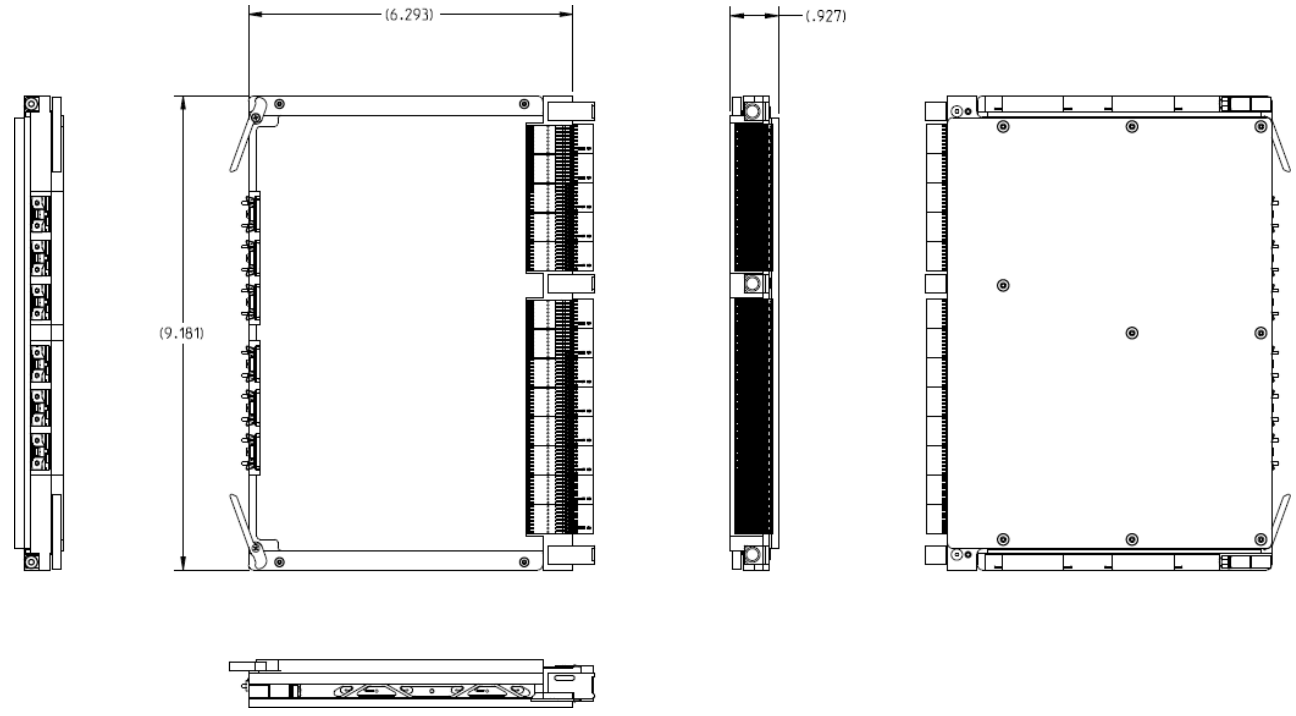
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Frame Components

The primary and secondary frame components are finished in accordance with MIL-DTL-5541 Type II, Class 3 on aluminum alloy. Additional materials and finishes are available upon request.

Extraction Levers

The extraction lever is crafted from 7075-T7351 aluminum alloy and treated with a black anodized finish per MIL-A- 8625 Type II, Class 2 specifications.

Wedgelocks

We utilize a variety of wedgelocks per customer requirements, with our standard being the SW5T-475 series from WaveTherm. These wedgelocks are constructed from 6061-T6511 aluminum alloy and black anodized in compliance with MIL-A-8625 Type II, Class 2. They feature 300-series stainless steel fasteners, passivated per AMS2700.

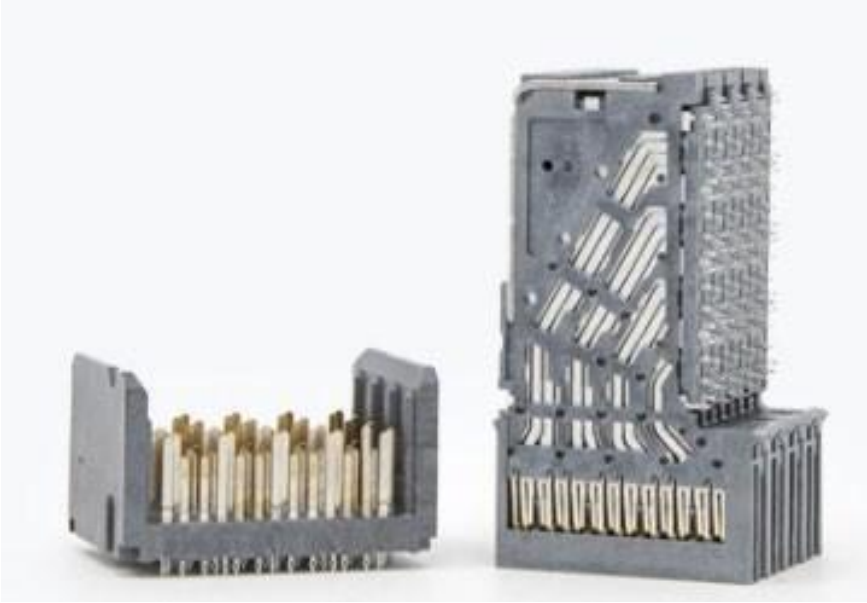
Labeling

Each board is equipped with an identification label, an ESD label, and is protected by a clear overlay.

Board Variants with SOSA VITA91 Connectors

Amphenol has designed these connectors in alignment with The Open Group Sensor Open Systems Architecture™ (SOSA) technical standard, MIL-HD2 provides developers with a readily available, robust open architecture solution for tighter card pitches and chassis designs where space requirements and density are critical. These connectors are available in 3-, 4-, and 6-pair configurations, providing the MIL-embedded market with the highest count of differential pairs available today in a 3U configuration at 56Gb/s PAM 4 speeds. This series was selected by the SOSA Consortium and provides a SOSA aligned solution for nextgen switch and payload card requirements enabling the MIL-embedded market to meet next-gen performance levels while still meeting COTS requirements.

- Highest density with 1.80mm pitch
- 4 diff, 8 column - SOSA aligned configuration
- Data rates scalable to 56Gb/s PAM4 to support system upgrades without costly redesigns
- Proprietary crosstalk reducing technologies
- 15.7mil drill compliant pin allows deeper backdrilling
- Optimized footprints
- Shielded contacts mate before signal contacts, providing up to a 4mm minimum wipe
- Embedded capacitor available
- Differential pairs 28-84 per inch (11-33 differential pairs per centimeter)
- Proven EMI and signal integrity advantages
- Improved impedance matching
- Complete solution for unique customer requirements
- Enables hot plugging
- Meets high density application requirements



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Amphenol Ruggedization Pedigree

OVERVIEW:

Amphenol integrated electronic products are designed and manufactured to our Ruggedization guidelines listed below. These guidelines ensure years of reliable operation in harsh environment applications where extreme operating temperatures, shock, vibration, and corrosive atmospheres are regularly experienced. Unless otherwise noted, the parts conform to the below specifications

TEMPERATURE:

- Operating Temperature- Thermal Cycles between -40°C and 85°C while device is operating
- Temperature is measured at chassis housing or card edge
- Storage Temperature- Thermal Cycles between -55°C and 125°C

HUMIDITY:

- Operating Humidity- Humidity cycle between 0-100% non-condensing humidity while device operating
- Storage Humidity- Humidity cycle between 0-100% condensing humidity

SEALING:

- Sealing can be optionally provided at the MIL-DTL-38999 interface with up to 10-5 cc/sec performance

SHOCK AND VIBRATION:

- Sine Vibration - 10g Peak, 5-2,000Hz
  - Based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 5 to 44 Hz, depending on specific test.
- Random Vibration - 0.0005 @ 5Hz, 0.1 @ 15 Hz, 0.1 @ 2,000 Hz
  - 60 minutes per axis, in each of three mutually perpendicular axes.
- 40 G Peak Shock Cycle
  - Three hits in each axis, both directions, ½ sine and terminal-peak saw tooth, Total 36 hits.

LUIDS SUSEPTABILITY:

- MIL-DTL-38999 receptacle interface per EIA-364-10E

ALTITUDE:

- -1,500 to 60,000 ft Altitude Testing w/ Rapid Depressurization

ELECTRONMAGNETIC COMPATIBILITY:

- Designed to comply with MIL-STD-461E

PRINTED CIRCUIT BOARD ASSEMBLIES:

- Conformal Coat
- Amphenol performs Conformal Coting to both sides of printed circuit board assemblies using HUSMISEAL IB31 in accordance with IPC-610, Class 3.
- Printed Circuit Board Rigidity
- Amphenol printed circuit boards are fabricated in accordance with IPC-6012, Class 3.
- Printed Circuit Board Fabrication
- Amphenol printed circuit boards acceptance criteria is in accordance with IPC-610, Class 3.

RELIABILITY PREDICTIONS (MTBF):

Amphenol can perform Mean Time Between Failure (MTBF) reliability analysis in full compliance with MIL-HDBK-217F-1 Parts Count Prediction and MIL- HDBK-217F-1 Parts Stress Analysis Prediction. We can also perform reliability analyses in full compliance of ANSI/ VITA 51.1 if it is required or preferred over the later met.

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