Amphenol
MILITARY HIGH SPEED

Fiber Optic Convection Cooled Ethernet Switch

168-Channel 25G/100G

PDS - 374



DESCRIPTION

Amphenol's rugged 168-channel 25G/100G Fiber Optic Convection Cooled Ethernet switch box offers configurable system connectivity, supporting a variety of speeds, port types, and seamless integration with high-speed media converters and connectors. Additionally, the switch is capable of supporting 1G, 10G, and 40G speeds.

Featuring 168 multi-mode fiber optic ports, each supporting up to 25G Ethernet, this switch undergoes rigorous testing at Amphenol's state-of-the-art communications testing center. It is tested at line rates in accordance with RFC 2889 for switching and RFC 2544 for Layer 2/Layer 3 performance, including metrics such as latency, packet forwarding, and other key performance indicators.

The switch is built using Amphenol's MIL-DTL-38999 Series connectors, incorporating standard AS39029-qualified Size 22D contacts, Octonet contacts, and 48F MT Ferrule Fiberoptic contact assemblies. For fiber optic Ethernet ports, Amphenol employs advanced MT ferrules, while the MT 38999-style contacts are utilized for power input and management functions.

FEATURES & BENEFITS

- 168 channels of up to 25G fiber Ethernet
- 28V MIL-STD-704 input module; MFM and DC/DC mil-spec power supply with hold-up capacitor and in-rush current limiting circuit.
- Built-in test functionality for power up, initiated, and continuous operation.
- Link status on demand, port counter status, configurable port speed/routing, ARP list, drop report, ping, MTU configuration, LUA configuration
- Power connector, debug connector, maintenance connector – all D38999's
- Mil-Spec black painted chassis with cold plate external conduction cooling

Part Number	Description
CF-02WA00-33X	**168-channel 25G fiber Ethernet switch box**

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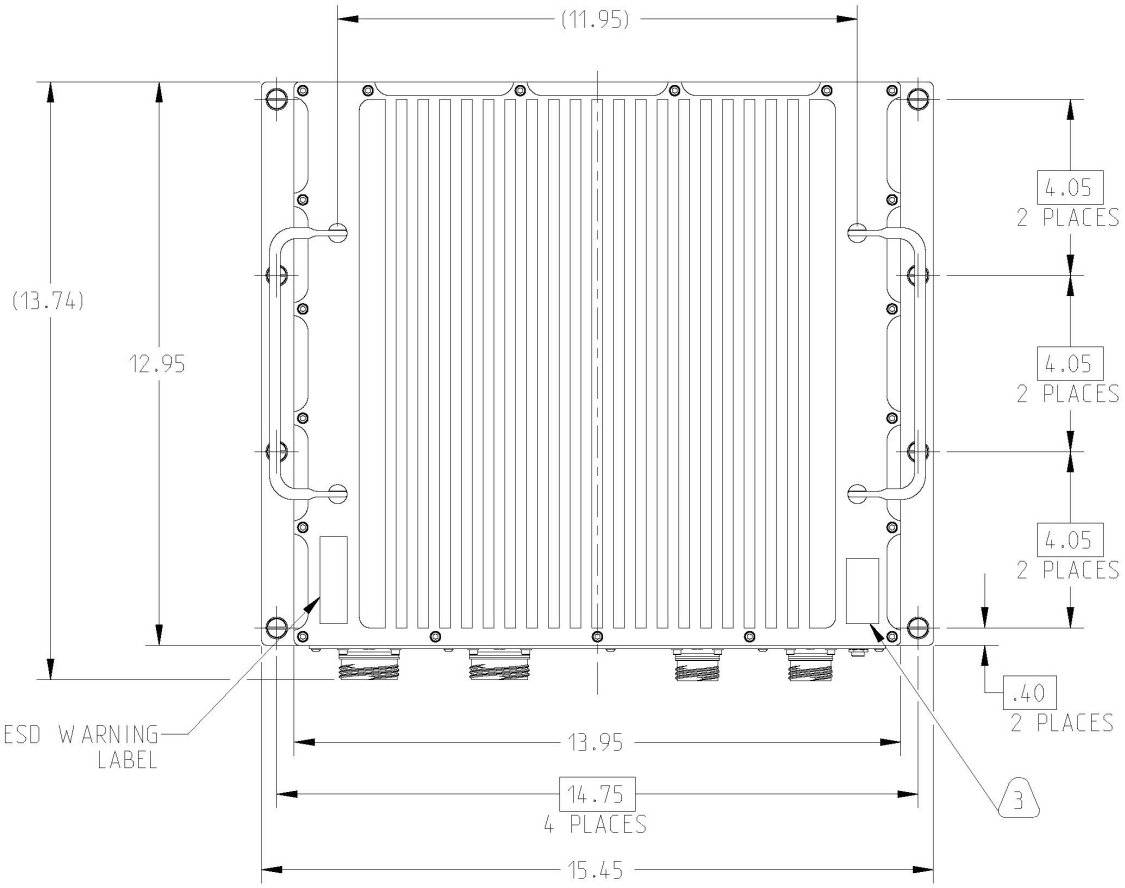
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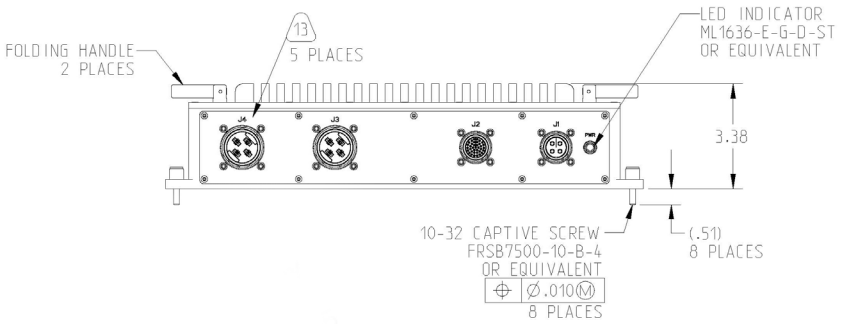
SOFTWARE FEATURES

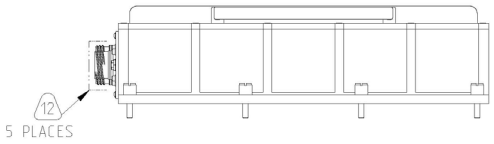
- **Stacking**
- Stacking Ring Topology
- Stacking Chain Topology
- Stacking Members and Unit ID
- Removing and Replacing Stacking Members
- Exchanging Stacking Members
- Switching the Stacking Master
- **Configuring System Time**
- Configuring Daylight Savings Time
- Configuring SNTP
- Polling for Unicast Time Information
- Polling for Anycast Time Information
- Broadcast Time Information
- Defining SNTP Settings
- **Configuring Device Security**
- Configuring Management Security
- Configuring Authentication Methods
- Defining Access Profiles
- Defining Profile Rules
- Defining Authentication Profiles
- Mapping Authentication Methods
- Defining RADIUS Settings
- Defining TACACS+ Authentication
- Configuring Passwords
- Defining Local Users
- Defining Line Passwords
- Defining Enable Passwords
- Configuring Network Security
- Network Security Overview
- Port-Based Authentication
- Advanced Port-Based Authentication
- Defining Port Authentication Properties
- Defining Port Authentication
- Configuring Multiple Hosts
- Defining Authentication Hosts
- Viewing EAP Statistics
- Defining Access Control Lists
- Defining IP Based Access Control Lists
- Defining MAC Based Access Control Lists
- Binding Device Security ACLs
- Managing Port Security
- Enabling Storm Control
- **Configuring System Logs**
- Defining General Log Properties
- Viewing Memory Logs
- Viewing Flash Logs
- Defining System Log Servers
- **Configuring Interfaces**
- Configuring Ports
- Aggregating Ports
- Configuring LACP
- Configuring VLANs
- Defining VLAN Properties
- Defining VLAN Membership
- Defining VLAN Interface Settings
- Configuring GARP
- Defining GARP
- Defining GVRP
- Viewing GVRP Statistics
- **Defining IP Addresses**
- Configuring IP Addressing
- Defining IP Addresses
- Defining ARP
- Defining Domain Name Servers
- Defining DNS Servers
- Defining DNS Host Mapping
- **Defining the Forwarding Database**
- Defining the Forwarding Database
- Defining Access Profiles
- **Configuring Spanning Tree**
- Defining Classic Spanning Tree
- Defining STP on Interfaces
- Defining Rapid Spanning Tree
- Defining Multiple Spanning Tree
- Defining MSTP Instance Settings
- Defining MSTP Interface Settings
- **Configuring SNMP**
- SNMP v1 and v2c
- SNMP v3
- Configuring SNMP Security
- Defining SNMP Security
- Defining SNMP View
- Defining SNMP Group Profiles
- Defining SNMP Group Members
- Defining SNMP Communities
- SNMP Communities Basic Table
- SNMP Communities Advanced Table
- Configuring SNMP Notifications
- Defining SNMP Notification Global Parameters
- Defining SNMP Notification Filters
- Defining SNMP Notification Recipients
- SNMPv1,2c Notification Recipients
- SNMPv3 Notification Recipients
- **Configuring Multicast Forwarding**
- Multicast Forwarding
- Typical Multicast Setup
- Multicast Operation
- Multicast Registration
- Multicast Address Properties
- Defining Multicast Properties
- Adding MAC Group Address
- Adding IP Multicast Groups
- Configuring IGMP Snooping
- Configuring MLD Snooping
- Viewing IGMP/MLD IP Multicast Groups
- Defining Multicast Router Ports
- Defining Forward All Multicast
- Defining Unregistered Multicast Settings
- **Managing System Files**
- Downloading System Files
- Firmware Download
- Configuration Download
- Uploading System Files
- Upload Type
- Software Image Upload
- Configuration Upload
- Copying Files
- Restoring the Default Configuration File
- **Configuring Quality of Service**
- Quality of Service Overview
- VPT Classification Information
- CoS Services
- Defining General QoS Settings
- Configuring QoS General Settings
- Restoring Factory Default QoS Interface Settings
- Defining Queues
- Defining Bandwidth Settings
- Mapping CoS Values to Queues
- Mapping DSCP Values to Queues
- Defining QoS Basic Mode
- Defining Basic Mode Settings
- Rewriting Basic Mode DSCP Values
- Defining QoS Advanced Mode
- Setting Policy Binding
- **Managing Device Diagnostics**
- Configuring Port Mirroring
- **Viewing Statistics**
- Viewing Interface Statistics
- Viewing Interface Statistics
- Receive Statistics
- Transmit Statistics
- Viewing Etherlike Statistics
- Managing RMON Statistics
- Viewing RMON Statistics
- Configuring RMON History
- Defining RMON History Control
- Viewing the RMON History Table
- Configuring RMON Events
- Defining RMON Events Control
- Viewing the RMON Events Logs
- Defining RMON Alarms

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DIMENSIONAL INFORMATION







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Pinout Chart

I/O CHART			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J1 (POWER) 15-4P KEYING "N"	A	IN	28VDC_IN
	B	OUT	28VDC_RTN
	C	--	SAFETY GROUND / CHASSIS
	D	--	NOT CONNECTED
	SHELL	--	CHASSIS

I/O CHART			
CONNECTOR DESCRIPTION	PIN NO.	DATA DIRECTION	SIGNAL NAME
J2 (DEBUG) 15-35P KEYING "N"	1	OUT	RS232_CONSOLE_TX
	2	IN	RS232_CONSOLE_RX
	3	--	GND
	4	--	N/C
	5	--	N/C
	6	--	GND
	7	BI	SWITCHBOX_RESET
	8	--	GND
	9	--	N/C
	10	--	N/C
	11	--	GND
	12	BI	DEBUG1_1GBase-T_DA+
	13		DEBUG1_1GBase-T_DA-
	14		DEBUG1_1GBase-T_DB+
	15		DEBUG1_1GBase-T_DB-
	16		DEBUG1_1GBase-T_DC+
	17		DEBUG1_1GBase-T_DC-
	18		DEBUG1_1GBase-T_DD+
	19		DEBUG1_1GBase-T_DD-
	20	--	N/C
	21	--	GND
	22	--	N/C
	23	--	N/C
	24	--	N/C
	25	--	N/C
	26	--	N/C
	27	--	GND
	28	--	N/C
	29	--	N/C
	30	BI	DEBUG2_1GBase-T_DA+
	31		DEBUG2_1GBase-T_DA-
	32		DEBUG2_1GBase-T_DB+
	33		DEBUG2_1GBase-T_DB-
	34		DEBUG2_1GBase-T_DC+
	35		DEBUG2_1GBase-T_DC-
	36		DEBUG2_1GBase-T_DD+
	37		DEBUG2_1GBase-T_DD-
	SHELL	--	CHASSIS

I/O CHART

CONNECTOR DESCRIPTION	PIN NO	SIGNAL NAME	ETHERNET PORT NO
	A1	25GBase-SR_RX	12
	A2	25GBase-SR_RX	11
	A3	25GBase-SR_RX	10
	A4	25GBase-SR_RX	9
	A5	25GBase-SR_RX	8
	A6	25GBase-SR_RX	7
	A7	25GBase-SR_RX	6
	A8	25GBase-SR_RX	5
	A9	25GBase-SR_RX	4
	A10	25GBase-SR_RX	3
	A11	25GBase-SR_RX	2
	A12	25GBase-SR_RX	1
	A13	25GBase-SR_TX	12
	A14	25GBase-SR_TX	11
	A15	25GBase-SR_TX	10
	A16	25GBase-SR_TX	9
	A17	25GBase-SR_TX	8
	A18	25GBase-SR_TX	7
	A19	25GBase-SR_TX	6
	A20	25GBase-SR_TX	5
J3	A21	25GBase-SR_TX	4
	A22	25GBase-SR_TX	3
21-04S	A23	25GBase-SR_TX	2
	A24	25GBase-SR_TX	1
4X 48F MT	A25	25GBase-SR_RX	24
	A26	25GBase-SR_RX	23
KEYING "N"	A27	25GBase-SR_RX	22
	A28	25GBase-SR_RX	21
	A29	25GBase-SR_RX	20
	A30	25GBase-SR_RX	19
	A31	25GBase-SR_RX	18
	A32	25GBase-SR_RX	17
	A33	25GBase-SR_RX	16
	A34	25GBase-SR_RX	15
	A35	25GBase-SR_RX	14
	A36	25GBase-SR_RX	13
	A37	25GBase-SR_TX	24
	A38	25GBase-SR_TX	23
	A39	25GBase-SR_TX	22
	A40	25GBase-SR_TX	21
	A41	25GBase-SR_TX	20
	A42	25GBase-SR_TX	19
	A43	25GBase-SR_TX	18
	A44	25GBase-SR_TX	17
	A45	25GBase-SR_TX	16
	A46	25GBase-SR_TX	15
	A47	25GBase-SR_TX	14
	A48	25GBase-SR_TX	13

I/O CHART

CONNECTOR DESCRIPTION	PIN NO	SIGNAL NAME	ETHERNET PORT NO
	B1	25GBase-SR_RX	36
	B2	25GBase-SR_RX	35
	B3	25GBase-SR_RX	34
	B4	25GBase-SR_RX	33
	B5	25GBase-SR_RX	32
	B6	25GBase-SR_RX	31
	B7	25GBase-SR_RX	30
	B8	25GBase-SR_RX	29
	B9	25GBase-SR_RX	28
	B10	25GBase-SR_RX	27
	B11	25GBase-SR_RX	26
	B12	25GBase-SR_RX	25
	B13	25GBase-SR_TX	36
	B14	25GBase-SR_TX	35
	B15	25GBase-SR_TX	34
	B16	25GBase-SR_TX	33
	B17	25GBase-SR_TX	32
	B18	25GBase-SR_TX	31
	B19	25GBase-SR_TX	30
	B20	25GBase-SR_TX	29
J3	B21	25GBase-SR_TX	28
	B22	25GBase-SR_TX	27
21-04S	B23	25GBase-SR_TX	26
	B24	25GBase-SR_TX	25
4X 48F MT	B25	25GBase-SR_RX	48
	B26	25GBase-SR_RX	47
KEYING "N"	B27	25GBase-SR_RX	46
	B28	25GBase-SR_RX	45
	B29	25GBase-SR_RX	44
	B30	25GBase-SR_RX	43
	B31	25GBase-SR_RX	42
	B32	25GBase-SR_RX	41
	B33	25GBase-SR_RX	40
	B34	25GBase-SR_RX	39
	B35	25GBase-SR_RX	38
	B36	25GBase-SR_RX	37
	B37	25GBase-SR_TX	48
	B38	25GBase-SR_TX	47
	B39	25GBase-SR_TX	46
	B40	25GBase-SR_TX	45
	B41	25GBase-SR_TX	44
	B42	25GBase-SR_TX	43
	B43	25GBase-SR_TX	42
	B44	25GBase-SR_TX	41
	B45	25GBase-SR_TX	40
	B46	25GBase-SR_TX	39
	B47	25GBase-SR_TX	38
	B48	25GBase-SR_TX	37

I/O CHART

CONNECTOR DESCRIPTION	PIN NO	SIGNAL NAME	ETHERNET PORT NO
	C1	25GBase-SR_RX	60
	C2	25GBase-SR_RX	59
	C3	25GBase-SR_RX	58
	C4	25GBase-SR_RX	57
	C5	25GBase-SR_RX	56
	C6	25GBase-SR_RX	55
	C7	25GBase-SR_RX	54
	C8	25GBase-SR_RX	53
	C9	25GBase-SR_RX	52
	C10	25GBase-SR_RX	51
	C11	25GBase-SR_RX	50
	C12	25GBase-SR_RX	49
	C13	25GBase-SR_TX	60
	C14	25GBase-SR_TX	59
	C15	25GBase-SR_TX	58
	C16	25GBase-SR_TX	57
	C17	25GBase-SR_TX	56
	C18	25GBase-SR_TX	55
	C19	25GBase-SR_TX	54
	C20	25GBase-SR_TX	53
J3	C21	25GBase-SR_TX	52
	C22	25GBase-SR_TX	51
21-04S	C23	25GBase-SR_TX	50
	C24	25GBase-SR_TX	49
4X 48F MT	C25	25GBase-SR_RX	72
	C26	25GBase-SR_RX	71
KEYING "N"	C27	25GBase-SR_RX	70
	C28	25GBase-SR_RX	69
	C29	25GBase-SR_RX	68
	C30	25GBase-SR_RX	67
	C31	25GBase-SR_RX	66
	C32	25GBase-SR_RX	65
	C33	25GBase-SR_RX	64
	C34	25GBase-SR_RX	63
	C35	25GBase-SR_RX	62
	C36	25GBase-SR_RX	61
	C37	25GBase-SR_TX	72
	C38	25GBase-SR_TX	71
	C39	25GBase-SR_TX	70
	C40	25GBase-SR_TX	69
	C41	25GBase-SR_TX	68
	C42	25GBase-SR_TX	67
	C43	25GBase-SR_TX	66
	C44	25GBase-SR_TX	65
	C45	25GBase-SR_TX	64
	C46	25GBase-SR_TX	63
	C47	25GBase-SR_TX	62
	C48	25GBase-SR_TX	61

I/O CHART

CONNECTOR DESCRIPTION	PIN NO	SIGNAL NAME	ETHERNET PORT NO
	D1	25GBase-SR_RX	84
	D2	25GBase-SR_RX	83
	D3	25GBase-SR_RX	82
	D4	25GBase-SR_RX	81
	D5	25GBase-SR_RX	80
	D6	25GBase-SR_RX	79
	D7	25GBase-SR_RX	78
	D8	25GBase-SR_RX	77
	D9	25GBase-SR_RX	76
	D10	25GBase-SR_RX	75
	D11	25GBase-SR_RX	74
	D12	25GBase-SR_RX	73
	D13	25GBase-SR_TX	84
	D14	25GBase-SR_TX	83
	D15	25GBase-SR_TX	82
	D16	25GBase-SR_TX	81
	D17	25GBase-SR_TX	80
	D18	25GBase-SR_TX	79
	D19	25GBase-SR_TX	78
	D20	25GBase-SR_TX	77
J3	D21	25GBase-SR_TX	76
	D22	25GBase-SR_TX	75
21-04S	D23	25GBase-SR_TX	74
	D24	25GBase-SR_TX	73
4X 48F MT	D25	25GBase-SR_RX	96
	D26	25GBase-SR_RX	95
KEYING "N"	D27	25GBase-SR_RX	94
	D28	25GBase-SR_RX	93
	D29	25GBase-SR_RX	92
	D30	25GBase-SR_RX	91
	D31	25GBase-SR_RX	90
	D32	25GBase-SR_RX	89
	D33	25GBase-SR_RX	88
	D34	25GBase-SR_RX	87
	D35	25GBase-SR_RX	86
	D36	25GBase-SR_RX	85
	D37	25GBase-SR_TX	96
	D38	25GBase-SR_TX	95
	D39	25GBase-SR_TX	94
	D40	25GBase-SR_TX	93
	D41	25GBase-SR_TX	92
	D42	25GBase-SR_TX	91
	D43	25GBase-SR_TX	90
	D44	25GBase-SR_TX	89
	D45	25GBase-SR_TX	88
	D46	25GBase-SR_TX	87
	D47	25GBase-SR_TX	86
	D48	25GBase-SR_TX	85

I/O CHART			
CONNECTOR DESCRIPTION	PIN NO	SIGNAL NAME	ETHERNET PORT NO
J4 21-04S 4X 48F MT KEYING "A"	A1	25GBase-SR_RX	108
	A2	25GBase-SR_RX	107
	A3	25GBase-SR_RX	106
	A4	25GBase-SR_RX	105
	A5	25GBase-SR_RX	104
	A6	25GBase-SR_RX	103
	A7	25GBase-SR_RX	102
	A8	25GBase-SR_RX	101
	A9	25GBase-SR_RX	100
	A10	25GBase-SR_RX	99
	A11	25GBase-SR_RX	98
	A12	25GBase-SR_RX	97
	A13	25GBase-SR_TX	108
	A14	25GBase-SR_TX	107
	A15	25GBase-SR_TX	106
	A16	25GBase-SR_TX	105
	A17	25GBase-SR_TX	104
	A18	25GBase-SR_TX	103
	A19	25GBase-SR_TX	102
	A20	25GBase-SR_TX	101
	A21	25GBase-SR_TX	100
	A22	25GBase-SR_TX	99
	A23	25GBase-SR_TX	98
	A24	25GBase-SR_TX	97
	A25	25GBase-SR_RX	120
	A26	25GBase-SR_RX	119
	A27	25GBase-SR_RX	118
	A28	25GBase-SR_RX	117
	A29	25GBase-SR_RX	116
	A30	25GBase-SR_RX	115
	A31	25GBase-SR_RX	114
	A32	25GBase-SR_RX	113
	A33	25GBase-SR_RX	112
	A34	25GBase-SR_RX	111
	A35	25GBase-SR_RX	110
	A36	25GBase-SR_RX	109
	A37	25GBase-SR_TX	120
	A38	25GBase-SR_TX	119
	A39	25GBase-SR_TX	118
	A40	25GBase-SR_TX	117
	A41	25GBase-SR_TX	116
	A42	25GBase-SR_TX	115
	A43	25GBase-SR_TX	114
	A44	25GBase-SR_TX	113
	A45	25GBase-SR_TX	112
	A46	25GBase-SR_TX	111
	A47	25GBase-SR_TX	110
	A48	25GBase-SR_TX	109

I/O CHART			
CONNECTOR DESCRIPTION	PIN NO	SIGNAL NAME	ETHERNET PORT NO
J4 21-04S 4X 48F MT KEYING "A"	B1	25GBase-SR_RX	132
	B2	25GBase-SR_RX	131
	B3	25GBase-SR_RX	130
	B4	25GBase-SR_RX	129
	B5	25GBase-SR_RX	128
	B6	25GBase-SR_RX	127
	B7	25GBase-SR_RX	126
	B8	25GBase-SR_RX	125
	B9	25GBase-SR_RX	124
	B10	25GBase-SR_RX	123
	B11	25GBase-SR_RX	122
	B12	25GBase-SR_RX	121
	B13	25GBase-SR_TX	132
	B14	25GBase-SR_TX	131
	B15	25GBase-SR_TX	130
	B16	25GBase-SR_TX	129
	B17	25GBase-SR_TX	128
	B18	25GBase-SR_TX	127
	B19	25GBase-SR_TX	126
	B20	25GBase-SR_TX	125
	B21	25GBase-SR_TX	124
	B22	25GBase-SR_TX	123
	B23	25GBase-SR_TX	122
	B24	25GBase-SR_TX	121
	B25	25GBase-SR_RX	144
	B26	25GBase-SR_RX	143
	B27	25GBase-SR_RX	142
	B28	25GBase-SR_RX	141
	B29	25GBase-SR_RX	140
	B30	25GBase-SR_RX	139
	B31	25GBase-SR_RX	138
	B32	25GBase-SR_RX	137
	B33	25GBase-SR_RX	136
	B34	25GBase-SR_RX	135
	B35	25GBase-SR_RX	134
	B36	25GBase-SR_RX	133
	B37	25GBase-SR_TX	144
	B38	25GBase-SR_TX	143
	B39	25GBase-SR_TX	142
	B40	25GBase-SR_TX	141
	B41	25GBase-SR_TX	140
	B42	25GBase-SR_TX	139
	B43	25GBase-SR_TX	138
	B44	25GBase-SR_TX	137
	B45	25GBase-SR_TX	136
	B46	25GBase-SR_TX	135
	B47	25GBase-SR_TX	134
	B48	25GBase-SR_TX	133

I/O CHART			
CONNECTOR DESCRIPTION	PIN NO	SIGNAL NAME	ETHERNET PORT NO
J4 21-04S 4X 48F MT KEYING "A"	C1	25GBase-SR_RX	156
	C2	25GBase-SR_RX	155
	C3	25GBase-SR_RX	154
	C4	25GBase-SR_RX	153
	C5	25GBase-SR_RX	152
	C6	25GBase-SR_RX	151
	C7	25GBase-SR_RX	150
	C8	25GBase-SR_RX	149
	C9	25GBase-SR_RX	148
	C10	25GBase-SR_RX	147
	C11	25GBase-SR_RX	146
	C12	25GBase-SR_RX	145
	C13	25GBase-SR_TX	156
	C14	25GBase-SR_TX	155
	C15	25GBase-SR_TX	154
	C16	25GBase-SR_TX	153
	C17	25GBase-SR_TX	152
	C18	25GBase-SR_TX	151
	C19	25GBase-SR_TX	150
	C20	25GBase-SR_TX	149
	C21	25GBase-SR_TX	148
	C22	25GBase-SR_TX	147
	C23	25GBase-SR_TX	146
	C24	25GBase-SR_TX	145
	C25	25GBase-SR_RX	168
	C26	25GBase-SR_RX	167
	C27	25GBase-SR_RX	166
	C28	25GBase-SR_RX	165
	C29	25GBase-SR_RX	164
	C30	25GBase-SR_RX	163
	C31	25GBase-SR_RX	162
	C32	25GBase-SR_RX	161
	C33	25GBase-SR_RX	160
	C34	25GBase-SR_RX	159
	C35	25GBase-SR_RX	158
	C36	25GBase-SR_RX	157
	C37	25GBase-SR_TX	168
	C38	25GBase-SR_TX	167
	C39	25GBase-SR_TX	166
	C40	25GBase-SR_TX	165
	C41	25GBase-SR_TX	164
	C42	25GBase-SR_TX	163
	C43	25GBase-SR_TX	162
	C44	25GBase-SR_TX	161
	C45	25GBase-SR_TX	160
	C46	25GBase-SR_TX	159
	C47	25GBase-SR_TX	158
	C48	25GBase-SR_TX	157

I/O CHART			
CONNECTOR DESCRIPTION	PIN NO	SIGNAL NAME	ETHERNET PORT NO
J4 21-04S 4X 48F MT KEYING "A"	D	NO CONNECT	

Amphenol Ruggedization Design

OVERVIEW:

Amphenol integrated electronic products are designed and manufactured to our Ruggedization guidelines listed below. These guidelines ensure years of reliable operation in harsh environment applications where extreme operating temperatures, shock, vibration, and corrosive atmospheres are regularly experienced. Unless otherwise noted, the parts conform to the below specifications

TEMPERATURE:

- Operating Temperature- Thermal Cycles between -40°C and 85°C while device is operating
- Temperature is measured at chassis housing or card edge
- Storage Temperature- Thermal Cycles between -55°C and 125°C

HUMIDITY:

- Operating Humidity- Humidity cycle between 0-100% non-condensing humidity while device operating
- Storage Humidity- Humidity cycle between 0-100% condensing humidity

SEALING:

- Sealing can be optionally provided at the MIL-DTL-38999 interface with up to 10-5 cc/sec performance

SHOCK AND VIBRATION:

- Sine Vibration - 10g Peak, 5-2,000Hz
  - Based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 5 to 44 Hz, depending on specific test.
- Random Vibration - 0.0005 @ 5Hz, 0.1 @ 15 Hz, 0.1 @ 2,000 Hz
  - 60 minutes per axis, in each of three mutually perpendicular axes.
- 40 G Peak Shock Cycle
  - Three hits in each axis, both directions, ½ sine and terminal-peak saw tooth, Total 36 hits.

FLUIDS SUSEPTABILITY:

- MIL-DTL-38999 receptacle interface per EIA-364-10E

ALTITUDE:

- -1,500 to 60,000 ft Altitude Testing w/ Rapid Depressurization

ELECTRONMAGNETIC COMPATIBILITY:

- Designed to comply with MIL-STD-461E

PRINTED CIRCUIT BOARD ASSEMBLIES:

- Conformal Coat
- Amphenol performs Conformal Coting to both sides of printed circuit board assemblies using HUSMISEAL IB31 in accordance with IPC-610, Class 3.
- Printed Circuit Board Rigidity
- Amphenol printed circuit boards are fabricated in accordance with IPC-6012, Class 3.
- Printed Circuit Board Fabrication
- Amphenol printed circuit boards acceptance criteria is in accordance with IPC-610, Class 3.

RELIABILITY PREDICTIONS (MTBF):

Amphenol can perform Mean Time Between Failure (MTBF) reliability analysis in full compliance with MIL-HDBK-217F-1 Parts Count Prediction and MIL- HDBK-217F-1 Parts Stress Analysis Prediction. We can also perform reliability analyses in full compliance of ANSI/VITA 51.1 if it is required or preferred over the later method

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