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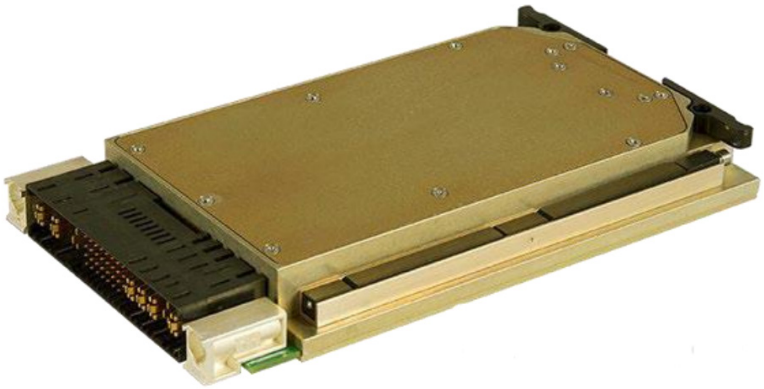
MILITARY HIGH SPEED

M4054 SERIES
DC/DC POWER SUPPLY



DESCRIPTION

The M4054 is a rugged, highly efficient, SOSA™ aligned, military grade 3U VPX, 1" pitch, 28V DC to DC PSU card that provides 12V and 3.3VAUX per VITA 62 and is capable of delivering up to 768W of output power. Features include: conduction cooling, current sharing, fast initialization, reverse battery protection, internal EMI filters, VITA 46.11 system management. The DC input range is 18-50V per MIL-STD-704 and DO-160, but variants support ranges of 12-100V per MIL-STD-1275 and Def Stan 61-5, part 6. The M4054 is field proven and is designed to meet MIL-STD-810, MIL-STD-461.

FEATURES

- VITA 62 Compliant
- Aligned with the SOSATM Technical Standard
- Wide input range
- Up to 800W output power[1]
- Remote sense
- Fixed switching frequency (220 kHz)
- External synchronization capability
- Indefinite short circuit Protection
- Over-voltage shutdown with auto-recovery
- Reverse battery protection
- Over temperature shutdown with auto-recovery
- EMI filters included
- System Management: protocol per VITA 46.11 Tier II
    - o Output voltages and currents
    - o Input voltage
    - o Card temperature
    - o Card system status

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HOW TO ORDER

PART NUMBER	CF-02EM4054	DC/DC Power Supply

PRODUCT SPECIFICATIONS:

DC Input	18 to 48VDC standard Max Non-Operation 100Vdc Options: 1) MIL-STD-704 (A-F) Normal and Abnormal Steady State 2) MIL-STD-704(A-F) transients Up to 50V, 80V. 3) MIL-STD-704(A-F) Transients Under 18V and Starting transients 4) MIL-STD-1275 Surges
DC Output	PO1 & PO3 (VS1): 12V up to 64A PO2 (3.3VAux): 3.3V up to 15A
Isolation	Over 20 MΩ at test voltage: 200V between Input and Output 200V between Input and Case 100V between Output and Case
EMC	Qualified to: MIL-STD-461G1 CE101, CE102, CS101, CS114, CS115, CS116 Notes: 1. Compliance achieved with 5µH LISN and static resistive load.
Line/Load Regulation	Ripple and Noise: Typically, less than 50mVp-p (max.1%p). Measured across a 0.1µF capacitor and 10µF capacitor on load at Input Voltage of 18V-36V, all Temperature Range.
Load Transient Overshoot and Undershoot	Output dynamic response of less than 5% at load Step of 30%-60%. Output returns to regulation in less than 1mSec
Normal Quiescent Current	Inhibited Output: 193mA (3.3VAux Only) Disabled Input: 112mA (All Outputs Off)
System management Options	1) I2C 2) Custom IPMI 3) VITA 46.11 Tier II IPMC Data available: Output voltages and currents, Input voltage, Card temperature, Card status

Environmental	Design to Meet MIL-STD-810G	
	Temperature	Operating: –55°C to +85°C at unit edge Storage: –55°C to +125°C Designed to meet 600 thermal cycles durability test
	Altitude	Method 500.5, Procedure I & II Storage/Air Transport: 40 kft Operation/Air carriage: 70 kft
	Salt Fog:	Method 509.5
	Fungus	Does not support fungus growth, in accordance with the guidelines of MIL- STD-454, Requirement 4
	Humidity	Method 507.5, Up to 95%
	Shock	Method 516.6 40g, 11msec saw-tooth (all directions)
	Vibration	Vibration: Figure 514.6E-1. General minimum integrity exposure. (1 hour per axis.)
Protections (Input)	**Inrush Current Limiter**	Peak value of 5 x IIN for initial inrush currents lasting more than 50µSec.
	Under Voltage	Unit shuts down when input steady state voltage drops below 17± 0.5VDC. Automatic restart when input voltage returns to nominal range. Low Line Transient TBD time protection is optional.
	Input Overvoltage Protection	Unit shuts down when inputsteady state voltage rise above 55/85 ± 2VDC.Automatic restart when input voltage returns to nominal range.
Protections (Output)	**Passive over voltage protection on 3.3VAux**	3.9V Zener.
	Active over voltage protection on 12Voutput	20% ± 5% above nominal voltage. Automatic recovery when output voltage drops below threshold.
	Overload / Short-Circuit protection	Continuous protection (10-30% above maximum current) for unlimited time (Hiccup). Automatic recovery when overload/short circuit removed.
Protections (General)	**Over Temperature Protection**	Automatic shutdown at internal temperature of 95 ± 5°C. Automatic recovery when temperature drops below 90 ± 5°C

Functions and Signals - According to VITA 62:

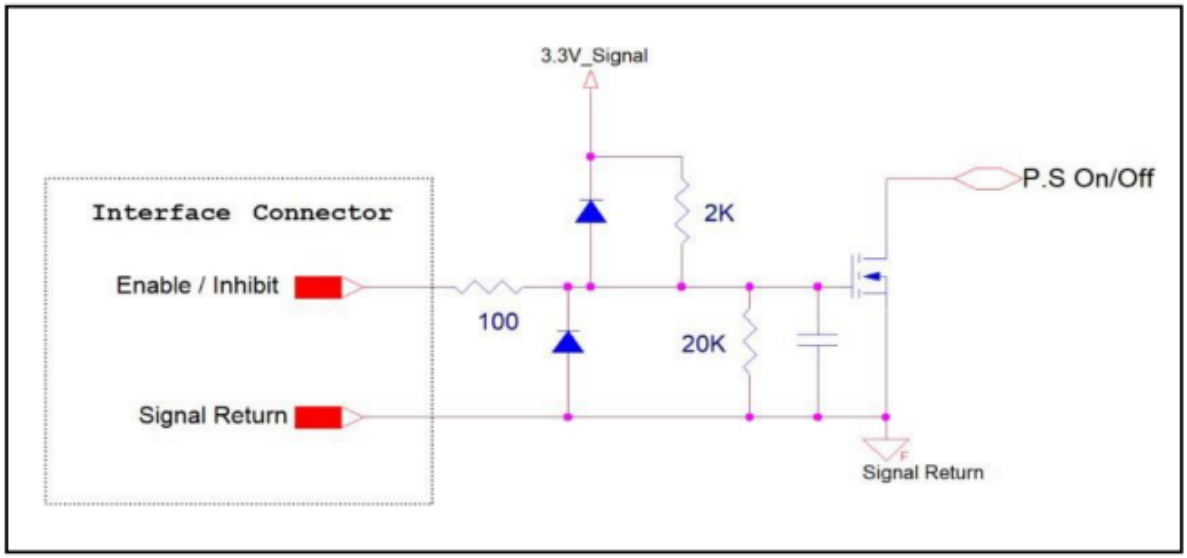
SIGNAL NAME	TYPE	DESCRIPTION
FAIL	Output	Indicates to other modules in the system that a failure has occurred in one of the outputs.
SYSRESET	Output	Indicates to other modules in the system that all outputs are within their working level.
INHIBIT	Input	Controls power supply outputs. This signal in conjunction with ENABLE controls the outputs.
ENABLE	Input	Controls power supply outputs. This signal in conjunction with INHIBIT controls the outputs.
GA0*, GA1*, GA2*	Input	Used for geographical addressing. GA2 is the most significant bit and GA0 is the least significant bit. [1]
SCL_A, SDA_A	Bidirectional	I2C bus Clock and Data respectively. Through this bus the voltage and temperature readouts can be shared. [1]
SCL_B, SDA_B	Bidirectional	Redundant I2C bus Clock and Data respectively. Through this bus the voltage and temperature readouts can be shared. [1]
Sync_In	Input	The Sync_In signal is used to allow the power supply frequency to sync with the system frequency. [1] Optional.
VOUT SENSE	Input	The SENSE is used to achieve accurate load regulations at load terminals (this is done by connecting the pins directly to the load's terminals).
3.3Vaux A.C.S	Bidirectional	Support 3.3Vaux Active current share between Outputs. See Current Share para. [1] [2] [3] (Optional, non-SOSA configuration)
PO#_SHARE	Bidirectional	Support current share between Outputs[1]

Notes:
1. Signal referenced to SIGNAL RTN.
2. When not used leave open
3 for 3.3Vaux In Passive or Non-Current Share configuration, this pin is Internally Disconnected

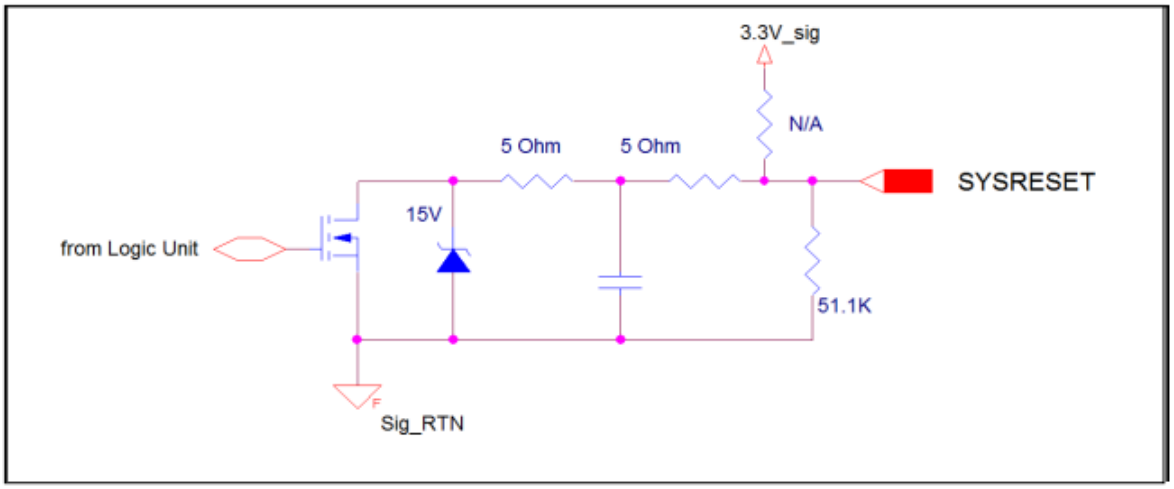
Inhibit and Enable Functionality

INHIBIT*	Low	Low	High	High
ENABLE*	Low	High	Low	High
VS1	OFF	OFF	ON	OFF
3.3V	ON	OFF	ON	OFF

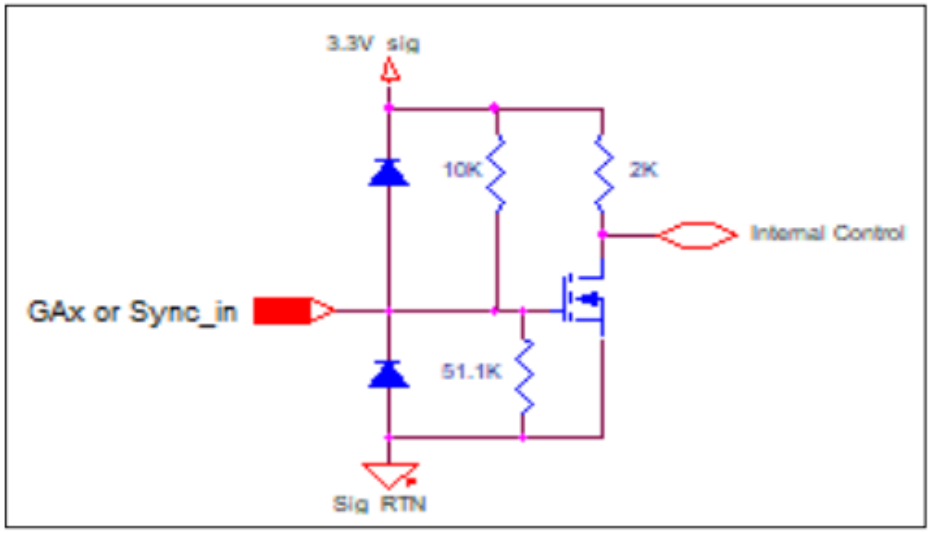
Inhibit and Enable Input stage



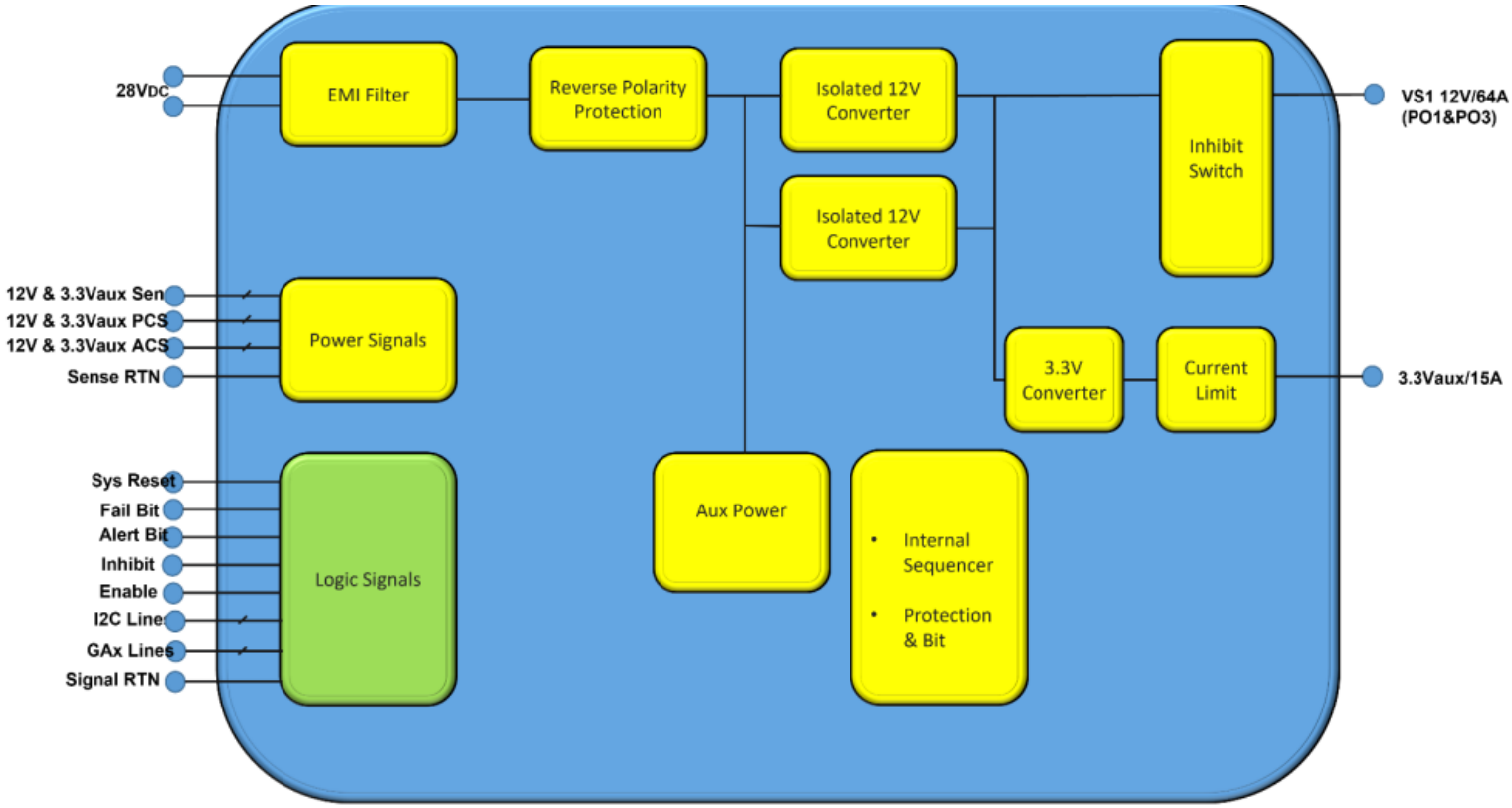
SysRst and Fail bit Output



GAx and Sync_In Stage



SIMPLIFIED BLOCK DIAGRAM:



DETAILED INFORMATION:

1.M4054 Input Voltage Operation.

The M4054 steady state operation voltage is 18V to 48V and will continuously work up to 50V/80V Input line. When configured to support MIL-STD 704/1275 transients or surges, the unit will shut down when input voltage rises above 60V or Under 16V for more than 2Sec and immediate shut down under 12V or above 100V Input. Power supply automatically recover when Input goes back to normal steady state line.

Please Note: Working at steady state low line under 22V may exceed connector 40A current limitation.
Unit can be calibrated to work steady state or to be limited by 10 Sec to support Input transients during low line.
If 10 Sec timer expired unit will turn off till input voltage goes back to 21V
Note: 1275E configuration is optional, contact Factory.

1.1 Steady state Low Line Turn-on and Turn-off Limits

To avoid Turn-on and Turn-off glitch the unit have about 3V Hysteresis. The Turn-on threshold is under 21V and turn- off
under 18V.
Those limits can be adjusted, contact Factory for more information.

2. Outputs VoltageRegulation

The M4054 contains accurate internal sense lines to keep output voltage at less than 4% regulation for all Line/ Load and temperature range (see Table).

Output Voltage Range	12V/64A	3.3V/15A
Active Current Share	11.85V - 12.15V	3.28V - 3.42V
Passive Current Share	N/A	3.25V - 3.45V

2.1 Sense Lines

Sense Lines are provided for VS1, VS2 and VS3 output to compensate line voltage drop. Sense Lines proper connection is shown in Figure 3.
Each VSx output has its own Sense Lines, additional common Sense RTN Line is provided for all VSx Outputs (VITA 62 Standard).

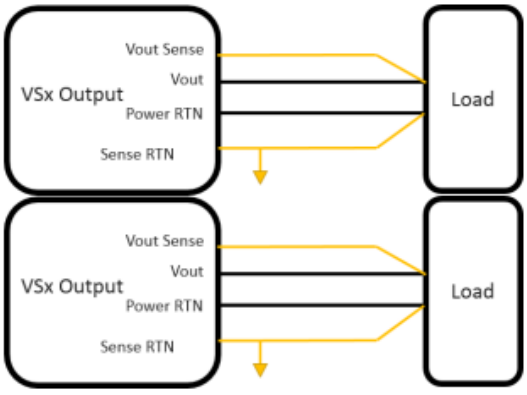


Figure 4: M4054 Sense line connection

3. Current Share (C.S)

Current Share of two or more units is optional (Contact Factory)
12V output and 3.3VAux will current share with about 2-4A load balance.

3.1 Active current sharing (A.C.S)

Current sharing done in a closed loop. All paralleled outputs are compared and feedback is used to balance their load current. The result is a more stable, less sensitive output voltage without voltage drop. Typical Load Balance of about 2-4A for all Load range is expected.
ACS is supported by the 12V output. Optional for 3.3Vaux[1] [2].

3.2 3.3Vaux Passive Current Sharing (P.C.S).

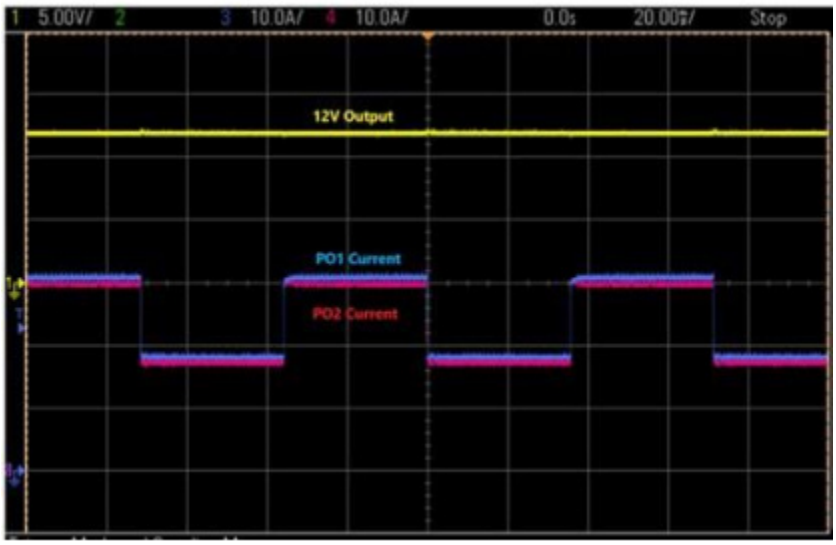
Current sharing is done in open loop, output voltage drops as a function of output load.
Load Balance of about 5-10% is expected.
3.3 Vaux ACS is optional[1] [2]

3.3Current share connection between two Units.

For a required output to current share please connect the following Pins between the two units

- PO#_Sense & PO#_Sense_RTN (for best performance, Pins from paralleled units should be connected to a single point and as close as possible to the load point)
- VS1_SHARE (A7)
- VS1_ ACS (C7)
- 3.3Vaux_SHARE (B7)
- 3.3Vaux_ACS (D1) Optional[1] [2]

Typical ACS Dynamic Load of Two 12V Paralleled Outputs (PO1 & PO2 refer to two different units)

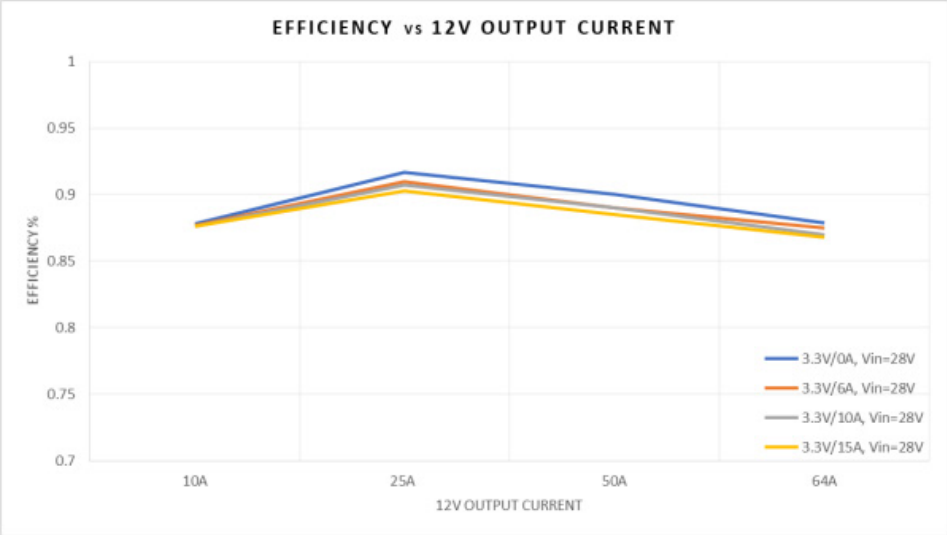


Notes 1. When Not used, 3.3Vaux A.C.S can be left open.

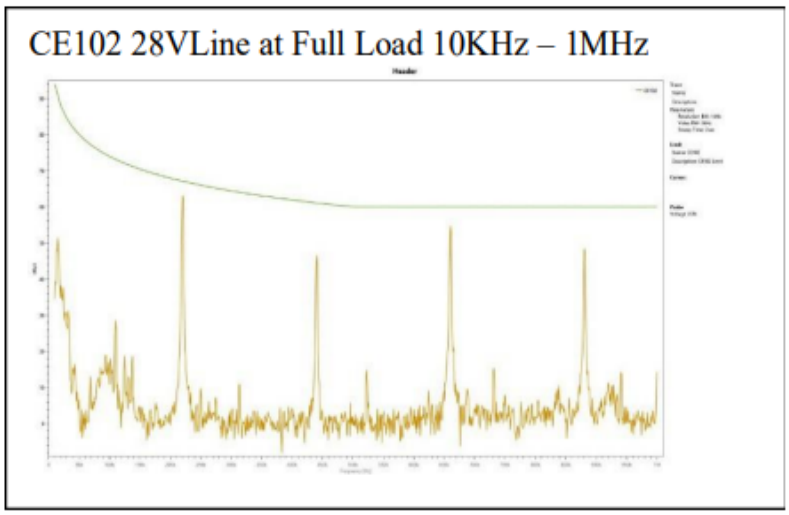
When ordering 3.3Vaux P.C.S or 3.3Vaux Non-Current Share unit, this pin is Internally disconnected

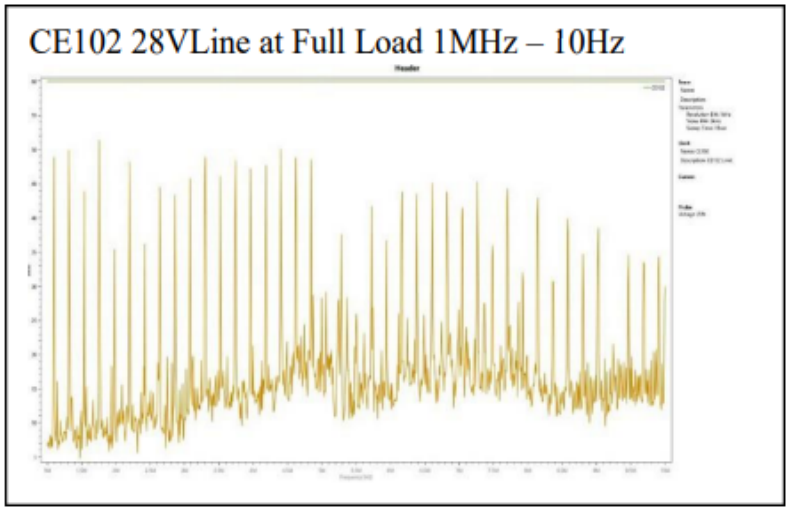
2. 3.3Vaux ACS (Pin D1) is not required by SOSA and is optional. (Pin was previously on Pin B4)

Efficiency



EMI CE102 Tests





6. Communication Protocol

Unit communication protocol can be configured as Vita 46.11 Tier 2 IPMC or Custom IPMI compatible protocol. For more details on protocols refer to para. 6.1 and 6.2

6.1 Custom IPMI Protocol

Electrical Parameters
Vcc: 3.3VDC
Pull-up: 20kOhm
Input capacitance: 100pf

Slave Device Addressing
- 256 address spaces
- Baud rate: 200kHz maximum
- 7 Bit Protocol
- Support Slot Addressing per VITA62

	MSB							LSB
Slot Number	A6	A5	A4	A3	A2/GA2*	A1/GA1*	A0/GA0*	R/W
Slot0	0	1	0	0	0	0	0	
Slot1	0	1	0	0	0	0	1	
Slot2	0	1	0	0	0	1	0	
Slot3	0	1	0	0	0	1	1	

Communications Supported

Read Command – 21Hex, deliver 64Bytes of Data. (More commands are available by request) The communication starts when the master sends a start followed by the unit slave address, command, checksum and a stop. A second start followed by the slave address and a read will be followed by a 64 Bites response.

S	Slave Address	R/W	A	Command	A	Check sum	A	P
	A6:A0	0	0	21 Hex	0	DF Hex	0	

W

S	Slave Address	R/	A	DATA	A	DATA	A	DATA	A	• • •	DATA	A	Check sum	N/A	P
	A6:A0	1	0	D7:D0	0	D7:D0	0	D7:D0	0		D7:D0	0	D7:D0	1	

Command – 21Hex read all 64 Bytes
S -Start
P- Stop

Master Transmit	Unit Transmit

Memory Space

Response Byte #	Data Type	Meaning	Interpretation	Reading Range
0	U Integer, MSB First	Echo of Command		21 Hex
1		N/A		00 Hex
2-3	S Integer, MSB First	Temperature -55C to 120C	T(C°)=+/- 7bit Dec	-55°C to 125°C
4-5	U Integer, MSB First	12V VS1 Voltage	V(out) = Data· m2	20.48V
6-7	U Integer, MSB First	3.3V VS2 Voltage	V(out) = Data· m2	20.48V
8-9	U Integer, MSB First	N/A	N/A	N/A
10-11	U Integer, MSB First	N/A	N/A	N/A
12-13	U Integer, MSB First	N/A	N/A	N/A
14-15	U Integer, MSB First	N/A	N/A	N/A
16-17	U Integer, MSB First	12V VS1 Current	V(out) = Data· m3	80A
18-19	U Integer, MSB First	3.3V VS2 Current	V(out) = Data· m3	20A
20-21	U Integer, MSB First	N/A	N/A	N/A
22-23	U Integer, MSB First	N/A	N/A	N/A
24-35	U Integer, MSB First	N/A	N/A	N/A
26-27	U Integer, MSB First	N/A	N/A	N/A
28-29	U Integer, MSB First	Reserved	00Hex	
30-31	U Integer, MSB First	Reserved	00Hex	
32-51	Character String (ASCII)	Part Number	M4054-xxx* (Note1)	20 Characters
52-53	Decimal, MSB First	Serial Number, 2MSB Dig	X,X Dec (Note2)	Optional
54-55	Decimal, MSB First	Serial Number, 2LSB Dig	X,X Dec (Note2)	Optional
56-57	Decimal, MSB First	Date Code	Week, Year (Note3)	Optional
58-59	Character String (ASCII)	Hardware Rev	B01 & B02 Boards (Note4)	2 Characters
60-61	Decimal, MSB First	Firmware Rev	X,X,X,X Dec (Note5)	4 digits
62	U Integer, MSB First	Reserved		AA Hex
63	U Integer, MSB First	Zero Checksum	Value required to make the sum of bytes 0 to 62 added to a multiple of 256	

Note:
M2 = 20.48/65535
M3 = 80/65535
M4 = 20/65535
*Matching unit part number

Notes 1 to 5

Note 1: Part Number Example: M4465

Byte No'	32	33	34	35	36	37	38	39-51
Character	M	4	4	6	5	(-)	4	0
Hex	4D	34	34	36	35	2D	34	00

Note 2: Serial Number Example: 25

Byte No'	52		53		54		55	
Dec Number	0	0	0	0	0	0	2	5
Binary	"0000"	"0000"	"0000"	"0000"	"0000"	"0000"	"0010"	"0101"

Note 3: Date Code Example: week 35 of 2018

Byte No'	56		57	
Dec Number	3	5	1	8
Binary	"0011"	"0101"	"0001"	"1000"

Note 4: Hardware Rev Example: B01 Rev (-), B01 Rev A

Byte No'	58	59
Character	(-)	A
Hex	2D	41

Note 5: Firmware Rev Example: 2.1.0.0

Byte No'	60		61	
Dec Number	2	1	0	0
Binary	"0010"	"0001"	"0000"	"0000"

6.2 46.11 Tier 2
Please see 46.11 User Manual for detailed information of operation.
Sensors included are seen in the table below.
Units are designed to be upgradable to 46.11 Tier 3 compliance upon release of that specification

Record ID	Sensor ID	Sensor Type	Name
0000	00	F0h	FRU State Sensor
0001	01	F1h	System IPMB Link Sensor
0002	02	F2h	FRU Health Sensor
0003	03	02h	FRU Voltage Sensor
0004	04	F3h	FRU Temperature Sensor
0005	05	F4h	Payload Test Results Sensor
0006	06	F5h	Payload Test Status Sensor
0100	07	02h	VS1 Voltage
0101	08	02h	VS2 Voltage
0106	0D	03h	VS1 Current
0107	0E	03h	VS2 Current
010C	13	01h	Analog Temperature
9090	N/A	N/A	Device Locator Record
9999	N/A	N/A	Device Management

7. Sync In and Switching Frequency

The unit free running switching frequency is 220KHz±5%
Unit can be synchronized to External clock signal in frequency range of 200KHz to 300KHz
External clock should be 3.3V CMOS standard logic level with duty cycle between 20% to 80%.
The Internal clock will sync after 32, within tolerance, external clock cycles.
Unit will revert to its internal clock upon any out of tolerance external clock and will require another 32 clocks to re synchronized.

Note: Synchronization function is optional, please contact factory if required.

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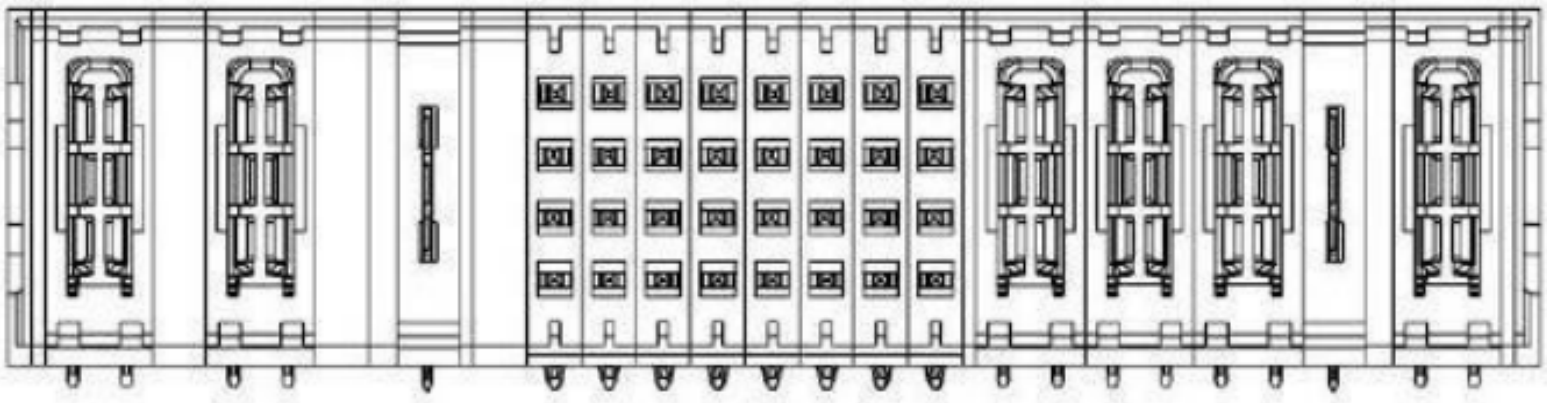
PART NUMBER	ROWS	POWER			SIGNAL								POWER				
		P1	P2	LP1	1	2	3	4	5	6	7	8	P3	P4	P5	LP2	P6
6450849-7	D	TT	TT	LT	Z5	Z5	Z5	Z5	Z5	Z5	Z5	Z5	TT	TT	TT	LT	TT
	C				Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5					
	B				R5	R5	R5	R5	R5	R5	R5	R5					
	A				05	05	05	05	05	05	05	01					
2ACP+1LP+32S+3HDP+1LP+1HDP																	



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Pin Assignments

Pin Number	Pin Name (12V only)	Pin functionality
P1	-DC_IN/ACN	-DC_IN
P2	+DC_IN/ACL	+DC_IN
LP1	CHASSIS	CHASSIS
P3	+12VDC (Vs1)	VS1
P4	POWER_RETURN	POWER_RETURN
P5	POWER_RETURN	POWER_RETURN
LP2	3.3V_AUX	3.3Vaux
P6	+12VDC (Vs1)	VS1
A8	SENSE, +12VDC	VS1_SENSE
B8	SENSE, 3.3V_AUX	3.3Vaux _SENSE
C8	SENSE, +12VDC	N.C (VS1_SENSE)
D8	SENSE_RETURN	SENSE_RETURN
A7	SHARE_1	VS1_SHARE
B7	SHARE_2	3.3Vaux _ SHARE
C7	SHARE_3	VS1_ACS
D7	SIGNAL RETURN	SIGNAL RETURN
A6	SM2	SCL_B
B6	SM3	SDA_B
C6	Reserved	N.C.
D6	SYSRESET*	SYSRESET*
A5	GA0*	GA0*
B5	GA1*	GA1*
C5	SM0	SCL_A
D5	SM1	SDA_A
A4	Reserved	N.C.
B4	Reserved	N.C.
C4	Reserved	N.C
D4	Reserved	N.C
A3	SYNC_IN (UD0)	N.C. (Sync_In)
B3	Reserved	N.C.
C3	NED	N.C (NED)
D3	NED_RETURN	N.C (NED RETURN)
A2	VBAT	N.C.
B2	FAIL*	FAIL*
C2	INHIBIT*	INHIBIT*
D2	ENABLE*	ENABLE*
A1	SYNC_OUT (UD1)	N.C.
B1	NVMRO (UD2)	N.C
C1	GA2* (UD3)	GA2*
D1	UD4	N.C. (3.3Vaux_ACS)

Notes:
1. Pin names N.C (function) are default not connected with optional
configuration per request.

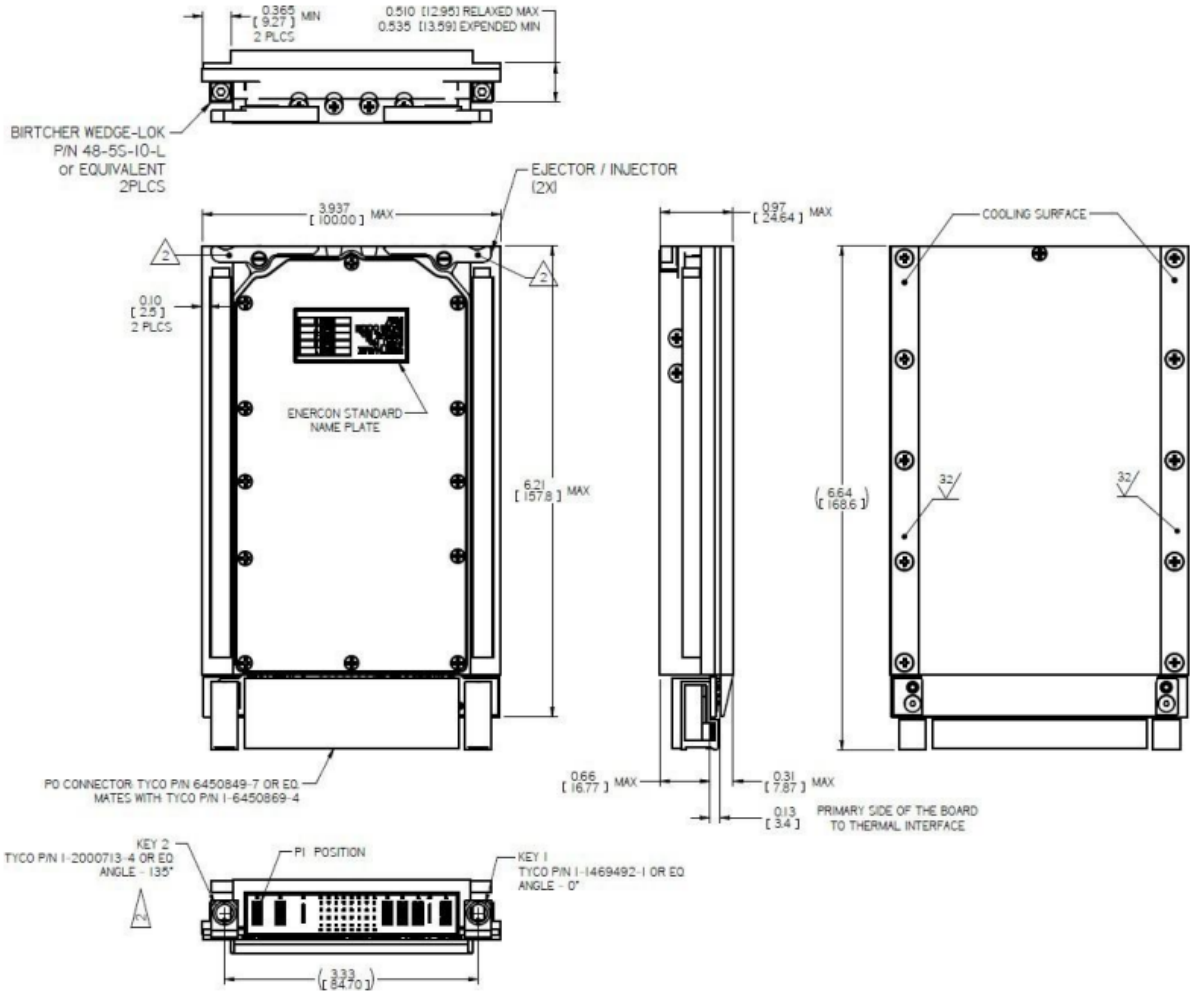
2. Pin B4 was previous configured as 3.3Vaux_ ACS.

3. Pin A1 was previous configured as Sync_In (labeled as Ref Clk (+))

4. Pin A3 was previous configured Ref_Clk (-) / N.C. and was unused

5. Pin D1 was previously labeled as Alert/N.C

OUTLINE DRAWING:



Notes
1. Dimensions are in Inches[mm]
2. Tolerance is:
.XX ±0.02 IN
.XXX ± 0.008 IN
3. Weight: Approx. 830g (29.28) oz
4. 3D model available

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