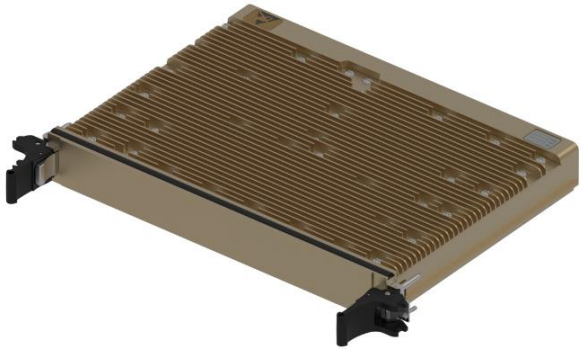
M4700 SERIES

AC/DC POWER SUPPLY



PRODUCT HIGHLIGHTS

- **VITA 62 COMPLIANT**
- **6U VPX FORM FACTOR**
- **AC/DC CONVERTER**
- **Up to 1000W Steady State**
- **Cyber Secure**

Description

M4700 is a military grade 6U VPX, VITA62 power supply that provides 12V, 5V and VAUX per VITA 62 that is rated at 1000W output power. Features include: Air Flow By cooling, 1.2" pitch, current-sharing, internal EMI filters, VITA 46.11 system management. AC input is 115V per MIL-STD-704. Designed to meet MIL-STD-810 and MIL-STD-461.

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Amphenol
MILITARY HIGH SPEED

M4700 Series– AC/DC Power Supply

Applications

Military (Airborne, ground-fix, shipboard), Ruggedized, Telecom, Industrial

Special Features

- VITA 62 6U 1.2”
- High efficiency
- Input / Output isolation
- Remote sense
- EMI filters included
- Fixed switching frequency
- Parallel configuration
- 46.11 Tier 2 communication
- External Inhibit & Enable
- Indefinite short circuit protection with auto-recovery
- Over temperature shutdown with auto recovery

Electrical Specifications

AC Input

115 VAC (Y)

- Works Through MIL-STD-704 (B-F) Normal and Abnormal Steady State.
- Works Through MIL-STD-704(B-F) Normal transients
- Protected MIL-STD-704(B-F) Abnormal Transients

Line/Load regulation

See Table 2 on page 6.

Ripple and Noise

Less than 50mV$_{p-p}$, typical (max. 1%), Under all Line, Load, and temperature condition (Line frequency 380 to 420Hz). measured across 0.1µF and 10µF on Load.

System Management Options

1) I2C
2) VITA 46.11 Tier II IPMC

Data available:

- Output voltages and currents
- Input voltage
- Card temperature
- Card status

DC Outputs

PO1&PO2	12V/60A
PO3	5V/30A
3.3Vaux	3.3V/20A
12Vaux	12V/1A
(-)12Vaux	(-) 12V/1A

Total Steady state Power 1000W (–55°C to +85°C Frame).

Power Factor

> 0.87 at 1kW

Current Share[3]

12V Active Current share
5V Active Current share

Load Transient

Output dynamic response up to 5% at step load of 30%-90%.
Output return to steady stated within 300-500µSec

Isolation

500V$_{DC}$ Input to Output
500V$_{DC}$ Input to Case
500V$_{DC}$ Output to Case

EMC

Designed to meet MIL-STD-461F [2]
CE102, CS101, CS114, CS115, CS116, CS117 & RE102

Efficiency

Typical 87% (Nominal line, nominal load, room temperature)

Notes:
[1] Contact Factory for peak power options.
[2] RE102 Supported at system Level.
[3] Current share is optional, default configuration does not support current share.

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Protections (Thresholds and protections can be modified / removed – please consult factory).

Input

- **Inrush Current Limiter**: peak value of 5 x I_{IN} for inrush currents lasting longer than 100µs.
- **Under Voltage Lock-Out** Unit shuts down when input voltage is below 70VAC ± 5VAC.
- **Catastrophic Failure Protection** Fuses are available to protect from catastrophic failure. The fuses are rated not to engage due to any normal type operation.

Outputs

- **Over Voltage Protection**: 12V latch & fused Zener
  5V latch & fused Zener
  3.3Vaux fused Zener
  12Vaux Hiccup
  (-)12Vaux fused Zener
- **Overload / Short Circuit Protection**
  12V, 5V Output-Continuos Hiccup protection (110-130%).
  3.3Vaux Hiccup protection (110-150%).
  12Vaux Hiccup (110-180%)
  (-)12Vaux Hiccup/foldback (110-180%)

General

Over temperature Protection:
Shutdown at internal temperature of +100 °C±5°C.
Recovery at +80 °C±5°C.
I2C temperature sensors are located on PCB and will have correlation to Heat sink depends on load and airflow.

Environmental

Designed to meet MIL-STD-810G and VITA 47

Temperature
Operating: –55°C to +85°C (Max +85°C Envelope).
Storage: –55°C to +125°C

Humidity
810G Method 507.5 & VITA 47 Para. 5.6, Up to RH 95%.

Reliability
> 314,000 hours, calculated per MIL-STD-217F Notice 2 at +65°C on unit chassis, Ground Fixed. (complete analysis is still required)

Altitude
810G Method 500.5, Procedure II (Operational) & VITA 47 para. 5.7 60,000 ft.

Vibration
810G Method 514.6 Procedure I. General minimum integrity exposure.
(1 hour per axis
& VITA 47 Vibration Class V3

Salt Fog
Method 509.5

Shock
810G Method 516.6 Procedure I & VITA 47 Shock Class OS2
Saw-tooth, 40g peak, 11ms

Fungus
Does not support fungus growth, in accordance with the guidelines of MIL – STD – 454, Requirement 4.

Environmental Stress Screening (ESS)

Including random vibration and thermal cycles is also available. **Please consult factory for details.**

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Functions and Signals (according to VITA 62.0)

Signal Name	Type	Description
FAIL*	Output	Indicates to other modules in the system that a failure has occurred in one of the outputs. Please refer to Figure 2
SYSRESET*	Output	Indicates to other modules in the system that all outputs are within [1] their working level. Please refer to Figure 2
INHIBIT*	Input	Controls power supply outputs. This signal in conjunction with ***Enable*** controls the outputs. Please refer to Table 1 and Figure
ENABLE*	Input	Controls power supply outputs. This signal in conjunction with **INHIBIT** controls the outputs. Please refer to Table 1 and Figure 1
GA0-4*, GAP*	Input	Used for geographical addressing. GA4 is the most significant bit and GA0 is the least significant bit.
SCL, SDA	Bidirectional	I2C bus Clock and Data respectively. Through this bus the voltage and temperature readouts can be shared.
Temperature BIT	Output	Indicates to other modules about input missing phase.
Missing Phase BIT	Output	Indicates to other modules about input missing phase.
VOUT SENSE	Input	The SENSE is used to achieve accurate load regulations at load terminals (this is done by connecting the pins directly to the load's terminals).
12VCS, 5VCS	Bidirectional	Support current share between Outputs. Two pins required. [1] [2]
12V ACS, 5V ACS	Bidirectional	Support Active current share between Outputs. See Current Share para. [1] [2]

Notes:

[1] All Signals referenced to **SIGNAL RTN**

[2] When not used leave open

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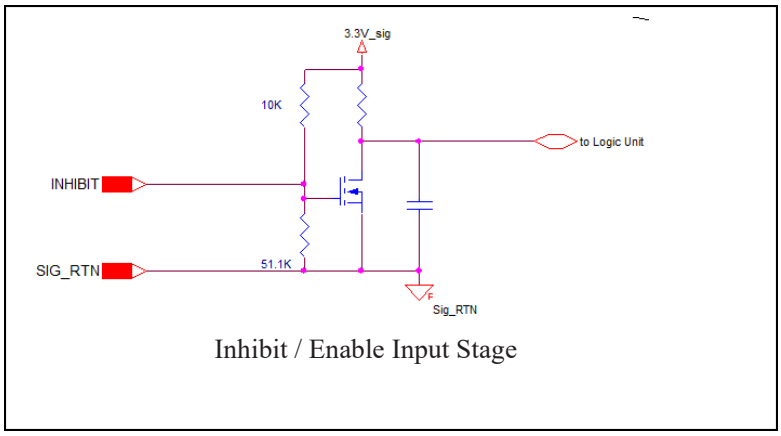
Table 1 – Inhibit and Enable Functionality

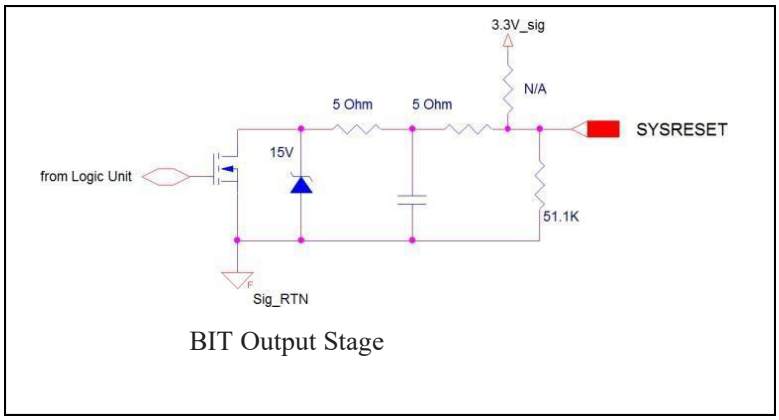
INHIBIT*	Low	Low	High	High
ENABLE*	Low	High	Low	High
All Outputs	OFF	OFF	ON	OFF
3.3V_AUX	ON	OFF	ON	OFF

Figure 1 – Inhibit and Enable Input stage



Inhibit / Enable Input Stage

Figure 2 –BIT Output Stage



BIT Output Stage

Detailed Information

1. Input Voltage Operation.

The M4700 steady state operation is per Mil-STD-704. Unit will work thorough all Normal Transients per Mil- STD-704 B to F, protected to all other transients and interrupts.

2. Outputs Voltage Regulation

The M4700 contains accurate internal sense lines to keep output voltage at less than 3% regulation for all Line / Load and temperature range (see Table 2).

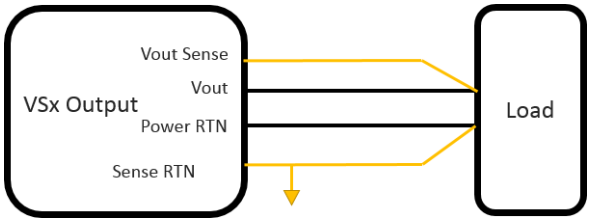
Output Voltage Range	12V/60A	5V/30A	3.3V/20A	12V/1A	(-)12V/1A
Voltage	11.85V ÷ 12.15V	4.90V ÷ 5.10	3.20V ÷ 3.40V	11.70V ÷ 12.20V	-11.70V ÷ -12.15V

Table 2: Outputs voltage regulation. no load to full load, low line to high line (–55°C to 85°C)

The M4700 contains 12V & 5V & 3.3V sense line pairs.
For proper operation, connect only a single sense line to the point of load regulation.
The same recommendation applies to the sense return line.

For proper current shared operation, connect a single sense line from each M4700 to the same point of load regulation.

Figure 3 – Sense Lines connection



Part number	Input	Outputs				
		VS1 & VS2	VS3	3.3VAux	12VAux	(-)12VAux
M4700-1	100-125VAC 3 Phase,380Hz- 420Hz	12V/60A	5V/30A	3.3V/20A	12V/1A	-12V/1A

Table 3: Standard configuration

3. Current Share (C.S, Optional)

Current Share of two or more units is optional (Contact Factory). VSx outputs will current share with about 2-4A load balance.

3.1 Active Current Sharing (A.C.S, Optional)

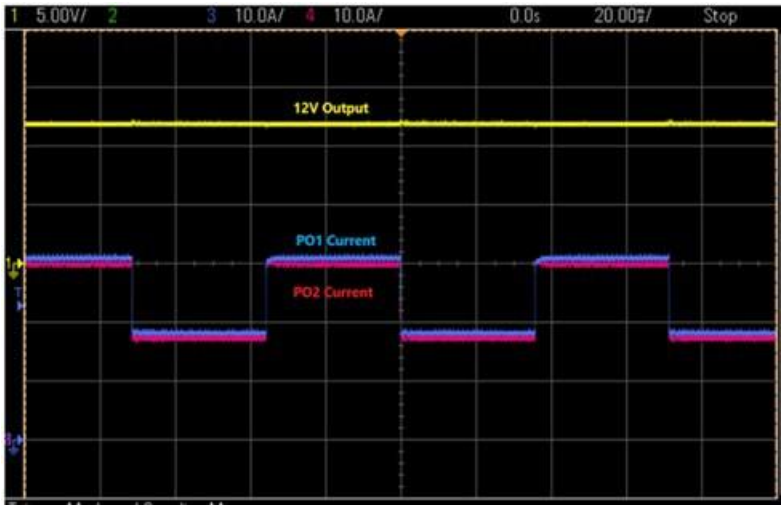
Current share done in a closed-loop. All paralleled outputs are compared and feedback is used to balance their load current. The result is a more stable, less sensitive output voltage without voltage drop. Typical Load Balance of about 1 to 4A for all Load range is expected.

3.2 Current share connection between two Units.

For a required output to current share please connect the following Pins between the two units

- **PO#_Sense** & **PO#_Sense_RTN** of each output should be connected to its corresponding output on the paralleled unit (for best performance, Pins from paralleled units should be connected to a single point and as close as possible to the load point).
- **VSx CS** of each output should be connected to its corresponding output on the paralleled unit.
- **VSx ACS** of each output should be connected to its corresponding output on the paralleled unit.
- In case two VSx have same output (E.g. VS1, VS2 are 12V), a single output can be connected and the other can be left open.
- When not used, share pins pins can be left open

Figure 4 -Typical ACS Dynamic Load of Two 12V Paralleled Outputs



4. Communication Protocol

Unit communication protocol can be configured as VITA 46.11 Tier 2 IPMC, VITA 46.11 Tier 1 IPMC or Advanced I2C protocol. For more details on protocols refer to para. 5.1 and 5.2

4.1 Advanced I2C Protocol

Electrical Parameters

Vcc	3.3VDC
Pull-up	20kOhm
Input capacitance	100pf

Slave Device Addressing

- 32 address spaces
- Baud rate: 200kHz maximum
- 7 Bit Protocol
- Support Slot Addressing per VITA 62

	MSB							LSB	
Slot Number	A6	A5/*GAP	A4/*GA41	A3/*GA3	A2/*GA2	A1/*GA1	A0/*GA0	R/W	GAP
Slot0	1	0	0	0	0	0	0		Short
Slot1	1	0	0	0	0	0	1		Open
Slot2	1	0	0	0	0	1	0		Open
Slot3	1	0	0	0	0	1	1		Short
Slot4	1	0	0	0	1	0	0		Open
…									
Slot31	1	0	1	1	1	1	1		Open

* Slot location is determined by GAx per VITA 62.

Communication Supported

Read Command – 21Hex, deliver 64Bytes of Data. (More commands are available by request) The communication starts when the master sends a start followed by the unit slave address, command, checksum and a stop. A second start followed by the slave address and a read will be followed by a 64 Bites response.

S	Slave Address	R/W	A	Command	A	Check sum	A	P
	A6:A0	0	0	21 Hex	0	DF Hex	0	

S	Slave Address	R/W	A	DATA	A	DATA	A	DATA	A	•••	DATA	A	Check sum	N/A	P
	A6:A0	1	0	D7:D0	0	D7:D0	0	D7:D0	0		D7:D0	0	D7:D0	1	

Command -21Hex read all 64 Bytes
S- Start
P-Stop

Master Transmit	Unit Transmit

Memory Space

Response Byte #	Data Type	Meaning	Interpretation	Reading Range
0	U Integer, MSB First	Echo of Command		**21 Hex**
1	U Integer, MSB First	N/A		**00 Hex**
2	S Integer, MSB First	Temperature	T(C°)=+/- 7bit Dec	**-55 to 125 °C**
3	U Integer, MSB First	Reserved	00Hex	
4-5	U Integer, MSB First	12V Voltage	V(out) = Data/ m2	**20.48V**
6-7	U Integer, MSB First	N/A	V(out) = Data/ m2	**"00"**
8-9	U Integer, MSB First	5V Voltage	V(out) = Data/ m2	**20.48V**
10-11	U Integer, MSB First	3.3V Aux Voltage	V(out) = Data/ m2	**20.48V**
12-13	U Integer, MSB First	12VAux Voltage	V(out) = Data/ m2	**Optional**
14-15	U Integer, MSB First	(-)12V Aux Voltage	V(out) = Data/ m2	**Optional**
16-17	U Integer, MSB First	12V Current	V(out) = Data/ m3	**80A**
18-19	U Integer, MSB First	N/A	V(out) = Data/ m3	**"00"**
20-21	U Integer, MSB First	5V Current	V(out) = Data/ m3	**40A**
22-23	U Integer, MSB First	3.3VAux Current	V(out) = Data/ m5	**20A**
24-35	U Integer, MSB First	12V Aux Current	V(out) = Data/ m4	**Optional**
26-27	U Integer, MSB First	(-)12V Aux Current	V(out) = Data/ m4	**Optional**
28-29	U Integer, MSB First	Reserved	00Hex	
30-31	U Integer, MSB First	Reserved	00Hex	
32-51	Character String (ASCII)	Part Number	M4700-xxx* (Note1)	**20 Characters**
52-53	Decimal, MSB First	Serial Number, 2MSB Dig	X,X Dec (Note2)	**Optional**
54-55	Decimal, MSB First	Serial Number, 2LSB Dig	X,X Dec (Note2)	**Optional**
56-57	Decimal, MSB First	Date Code	Week, Year (Note3)	**Optional**
58-59	Character String (ASCII)	Hardware Rev	B01 & B02 Boards (note4)	**2 Characters**
60-61	Decimal, MSB First	Firmware Rev	X,X,X,X Dec (Note5)	**4 digits**
62	U Integer, MSB First	Reserved		**AA Hex**
63	**U Integer, MSB First**	**Zero Checksum**	**Value required to make the sum of bytes 0 to 62 added to a multiple of 256**	

Note:
M_2=20.48 / 2^{16}-1
M_3=140 / 2^{16}-1
M_4=10 / 2^{16}-1
M_5=20 / 2^{16}-1
*Matching unit part number

Notes 1 to 5:

1. Part Number Example: M4065-4
2.

Byte No'	32	33	34	35	36	37	38	39-51
Character	M	4	0	6	5	(-)	4	0
Hex	4D	34	30	36	35	2D	34	00

3. Serial Number Example: 25

Byte No'	52		53		54		55	
Dec Number	0	0	0	0	0	0	2	5
Binary	"0000"	"0000"	"0000"	"0000"	"0000"	"0000"	"0010"	"0101"

4. Date Code Example: week 35 of 2018

Byte No'	56		57	
Dec Number	3	5	1	8
Binary	"0011"	"0101"	"0001"	"1000"

5. Hardware Rev Example: B01 Rev (-), B01 Rev A

Byte No'	58	59
Character	(-)	A
Hex	2D	41

6. Firmware Rev Example: 2.1.0.0

Byte No'	60		61	
Dec Number	2	1	0	0
Binary	"0010"	"0001"	"0000"	"0000"

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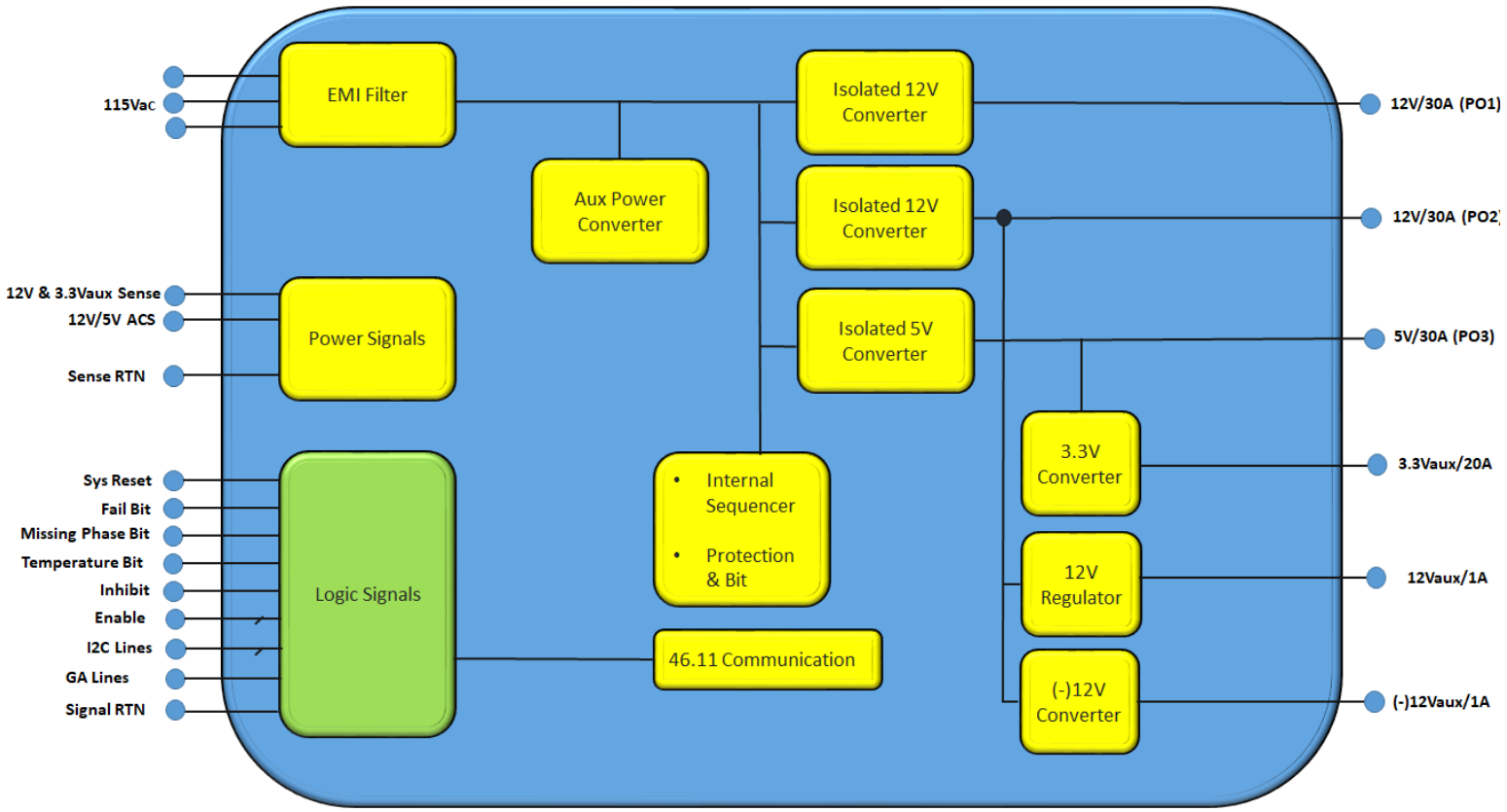
4.2 VITA 46.11 Tier 1 and Tier 2 IPMC

Please see 46.11 User Manual for detailed information of operation. Sensors included are seen in the table below.

Record ID	Sensor ID	Sensor Type	Name
0000	00	F0h	FRU State Sensor
0001	01	F1h	System IPMB Link Sensor
0002	02	F2h	FRU Health Sensor
0003	03	02h	FRU Voltage Sensor
0004	04	F3h	FRU Temperature Sensor
0005	05	F4h	Payload Test Results Sensor
0006	06	F5h	Payload Test Status Sensor
0100	07	02h	VS1 Voltage
0103	0A	02h	VS2 Voltage
0106	0D	02h	VS3 Voltage
0109	10	02h	3.3VAux Voltage
010C	13	02h	12VAux Voltage
010F	16	02h	(-)12VAux Voltage
0112	19	03h	VS1 Current
0115	1C	03h	VS2 Current
0118	1F	03h	VS3Current
011B	22	03h	12VAux Current
011E	25	03h	(-)12VAux Current
0121	28	01h	Analog Temperature
0122	29	01h	Analog Temperature 2
9999	N/A	N/A	Device Management

block diagram



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5. Pin Assignment

Connector P1: Connector type: 6450849-6 or eq

Pin Number	*Pin Name*
P10	12V/30A (VS1, VS2)
P9	12V/30A (VS1, VS2)
A9	12V_SENSE
B9	12V_SENSE
C9	5V_SENSE
D9	Missing Phase BIT
A8	12V_SENSE_RTN
B8	12V_SENSE_RTN
C8	5V_SENSE_RTN
D8	Temperature BIT
A7	12V_CS
B7	12V_ACS
C7	5V_CS
D7	SIGNAL_RETURN
P8	POWER_RETURN
P7	POWER_RETURN
A6	SCL_B
B6	SDA_B
C6	-12V_AUX
D6	SYSRESET*
A5	GAP*
B5	GA4*
C5	SCL
D5	SDA
A4	GA3*
B4	GA2*
C4	GA1*
D4	GA0*
A3	N.C
B3	+12V_Aux
C3	N.C
D3	N.C
P6	5V/30A
P5	5V/30A
P4	POWER_RETURN
P3	POWER_RETURN
A2	N.C
B2	FAIL*
C2	INHIBIT*
D2	ENABLE*
A1	N.C
B1	5V_ACS
C1	3.3Vaux Sense
D1	3.3Vaux Sense return
P2	3.3V/20A
P1	POWER_RETURN

Connector P0
Connector type: 2348886-1 or eq.

Pin Number	Signal Name
P7	PHASE A
P6	PHASE B
P5	PHASE C
P4	
P3	
P2	
P1	CHASSIS_GND

Notes:
• P5, P6 are shorted internally.
• P9, P10 are not shorted internally.
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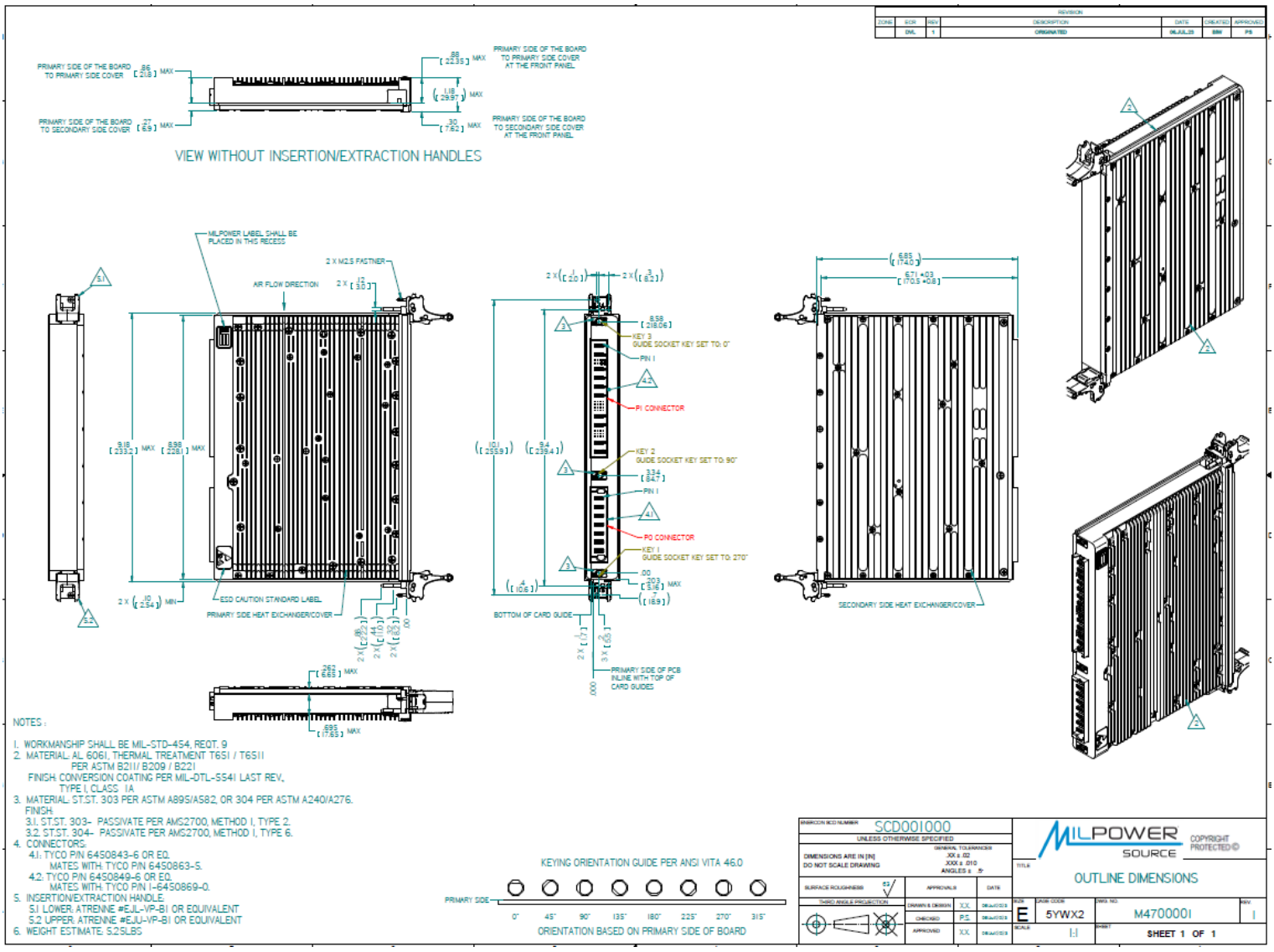
Outline Drawing

For detailed dimensions and tolerances see Drawing: M4700001



based on VITA 48.7 class B, No seals for Module to Backplane seal plate or Primary side cover to secondary side cover interface

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