M4054 SERIES

Power Supply Data Sheet

3U VPX 28V 800W - SOSA Aligned

VITA 47.1 CC4/CCW6 NT4 V3 OS2 C4 AV2 SF1/SF3 CS5

Product Highlight

- *Vita62 Compliant*
- *SOSA Alignment*
- *800W Steady State*
- *EMI Mil-STD-801G*
- *Operational Temperature -55°C to +85°C (unit Edge)*
  Input Options:
  - *Mil-STD-704*
  - *Mil-STD-1275 Transients*

John Tucci • Phone: (607) 563-5388 • Email: jtucci@amphenol-aao.com
• www.amphenol-aerospace.com

Amphenol
MILITARY HIGH SPEED

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1. Scope

The M4054 Power supply is a member of Milpower SOSA Aligned VPX product line and is intended to serve at 28V Input DC line to support a total of 800W steady state, under all Line and temperature conditions.

2. Module High Level Specification Details

Milpower Part Number **M4054**

Parameter	Functionality
Form factor	3U VPX, VITA 62 compliant 1" pitch
Cooling	Conduction cooled
Power input	28V Line, Mil-STD-704
Power output	12V/64A, 3.3V/15A, 800W Total.
Power Holdup	With M4162 unit.
Management	Tier-II IPMI/46.11 via P0 IPMI-A and (IPMI-B TBD) FPGA based management.
Temperature	-55C – 85C unit Edge (VITA 47.1 Extended CC4)
Weight	Approx 830g

2.1 Special Features

- VITA 62.0
- Aligned with the SOSA™ Technical Standard
- VITA 47.1 CC4/CCW6 NT4 V3 OS2 C4 AV2 SF1/SF3 CS5
- Wide Input Range
- Up to 800W output power without derating
- 12V Active Current share, 3.3V ACS or PCS
- Remote sense
- Outputs Short Circuit Protection
- Outputs Over Voltage Protection
- Over Temperature Shutdown with Auto Recovery
- Qualified Mil-STD-461-G (5µ LISN)
- System Management: protocol per VITA 46.11 (IPMI Tool, ELMA ChM)

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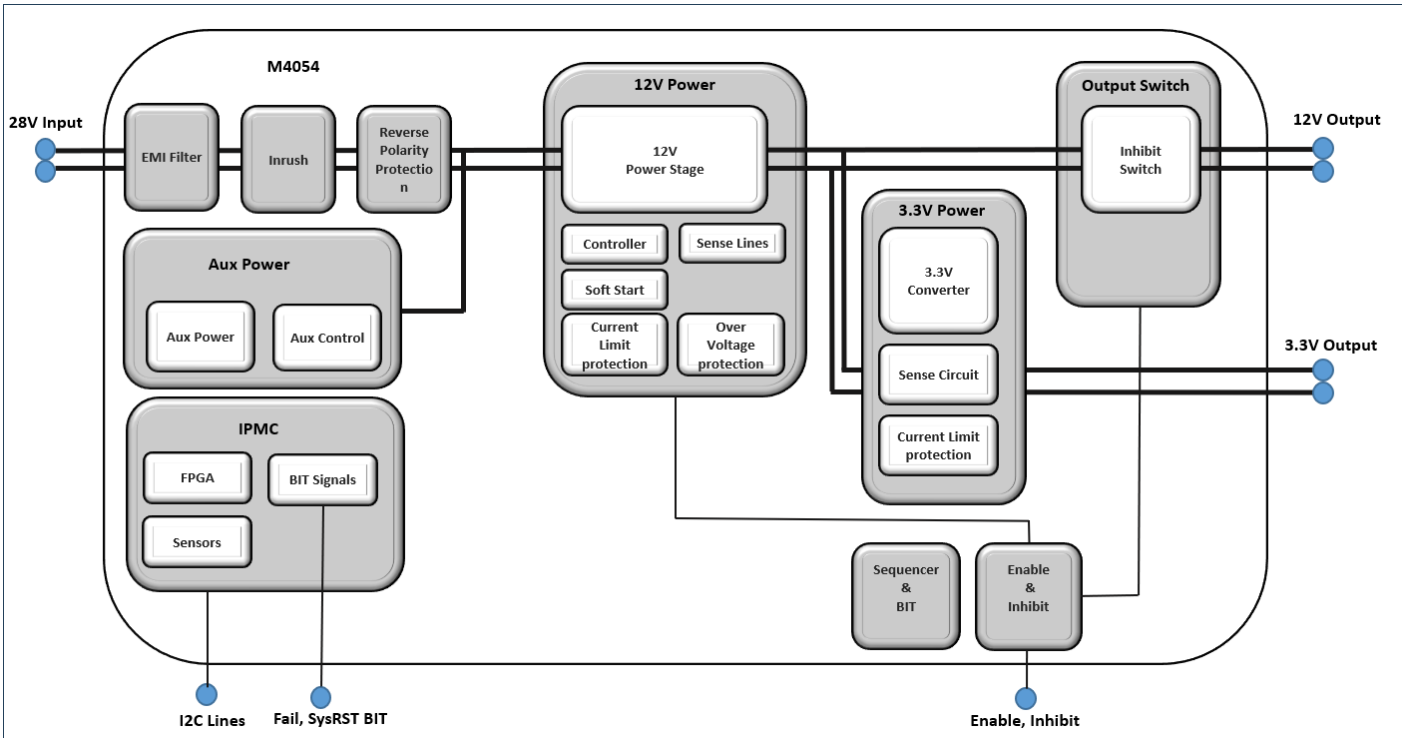
• www.amphenol-aerospace.com

3. M4054 Power Supply Operation

3.1 Unit Block Diagram



M4054 detailed block diagram

3.2 Electrical Specification

DC Input:	DC Outputs:	Isolation:
• 18V to 48V DC (Turn-on at Input voltage below 21V. Turn off below 18V line or after 10Sec under 22V Line) [1] • Optional: support All Over Voltage Transient Up to 100V Notes: 1. Full 704 Compliance at Sec 3.5.1.1 2. When Calling for LISN, 5µH is used	• VS1: 12V / 64A • 3.3Vaux: 3.3V / 15A	• 200V Input to Output & Chassis. • 100V Output to chassis

Line Load Regulation	Efficiency	EMC
• 12V Output 11.85V to 12.15V • 3.3V Output 3.28V to 3.42V, 3.25V to 3.45V parallel-PCS.	Up to 92%.	Mil-STD-461G 5µH LISN[1] CE101, CE102, CS101, CS114, CS114, CS115, CS116 Notes: All tests performed with Static resistive Load.
Ripple and Noise	**System Management Options:**	**Typical Quiescent Current**
Typical less than 50mV (max 1%). across 0.1µF capacitor with 10 µF on Load. Note: under all temperature range, Input voltage 18V to 36V.	• Advanced I2C Protocol • IPMC Tier 2 (Tier 3 Upgradable)	• Inhibited Output 290mA (28V Input, 3.3Vaux only). • Disabled Outputs 145mA (28V Input, Outputs Off).
Load Transients		
Outputs dynamic response less than 5% for Load steps 60% - 90%. Outputs returns to regulation <1mSec.		

3.2.1 Protections

Input Current Inrush:	Outputs Over Voltage	Over Load Protection:
• Bus capacitance ≈ 600µF. • Output Turn-on inrush Input current < 1A	• 12V Active OVP • 3.3Vaux 3.9V Zener	Hiccup Over-load / Short Circuit Protection. 12V typically, 103%-107% Load. 3.3V typically, 110%-130% Load.
Input Under /Over Voltage Protection	**Over Temperature Protection**	
• Turn-off above 50V. • Turn-off under 18V.	Thermal shutdown at Unit temperature of 90-105°C. Auto Recovery 90±5°C (unit Edge, wedge lock side)	

- Turn-off after 10Sec below 22V.
  Note: T.H can be modified.

3.3 Environmental Specification.

VITA 47.1 CC4/CCW6 NT4 V3 OS2 C4 AV2 SF1/SF3 CS5

Temperature:

- Operational -55C° to 85C° unit edge, -55C° to 71C° cold wall.
- Exceed Vita 47 CC4.
- Storage -55C° to 125C°
- Qualified 600 Thermal Cycles
  Note: Plug-in unit edge surface temperature is measured on the plug-in unit

Altitude:

Mil-STD-810G Method 500.5 procedure I & II

- Storage / Air Transport: 40kft
- Operation / Air carriage: 70kft

Rapid Decompression

Designed to meet per Vita 47.1

Corrosion Resistance

- Mil-STD-810G, Method 509.5.
- VITA47 Class SF1, SF3
- VITA47 Class SF2 TBD

Fungus

Does not support Fungus growth per Mil-HDBK-454, Guideline 4.

Humidity

- Mil-STD-810G, Method 507, up to 95% RH.
- Optional:100% condensation, consult factory.

Vibration & Shock

- Vita47 Vibration Class V3.
- Vita 47 Operational Shock Class OS2
- Vita 47 Bench Handling Shock (Connector not protected, may be damaged).

Reliability

481,000 Hours,
calculated IAW MIL-HDBK-217F Notice 2
at +65 ℃, GF

ESS

Environmental Stress Screening available, please contact factory for details

3.4 Unit Interfaces

3.4.1 Connectors

Front Panel Connector **Mating Connector**	Tyco 6450849-7 or equivalent Tyco 1-6450869-4 or equivalent	Main Connector Backplane Connector
Wedge Locks	48-5S-10-L or Equivalent	
Key 1 **Key 2**	0° 135°	
Back Panel USB-C Port	USB Type-C (Road map, M4055)	FPGA Programing Port

3.4.2 Functions and Signals

Signal Name	Type	Description
FAIL*	Output Open Drain	Indicates to other modules in the system that a failure has occurred in one of the outputs. [1,2] Normally Open.
SYSRESET*	Output Open Drain.	Indicates to other modules in the system that an output voltage is not in its nominal range. [1,2] Normally Open.
INHIBIT*	Input	Controls 12V Output. [1,3]
ENABLE*	Input	Controls 12V, 3.3V Outputs. [1,3]
GA0*, GA1*, GA2*	Input	System addressing per VITA46. [1]
SCL_A, SDA_A	Bi-Direction	Primary I2C lines. [1]
SCL_B, SDA_B	Bi-Direction	Secondary I2C lines. [1]
SYNC IN	Input	External Clock for PWM Synchronization. [1]
PO_SENSE	Output	Output Sense line for voltage compensation. [1]
SENSE RETURN	Output	Output Sense return for voltage compensation. Common line for all outputs.
SHARE	Bi-Directional	Current share pins
3.3V AUX ACS	Bi-Directional	Additional Current share pin to support 3.3VAux Active current share.
SIGNAL RETURUN	Passive	Return path for all signals, refers to Output Power ground.

Notes

1 Refers to SIGNAL RETURN

2 See para 3.5.3.1 for additional information

3 See para 3.5.2.1 for additional information

3.5 Power Detailed Description

3.5.1 Input Voltage

3.5.1.1 Operational Input Range

Unit will be fully operational under all steady state condition up to 50V line. Protection or operation through 80V and 100V transients is optional.
Turn -on voltage is under 21V volt, before going into normal steady state.
To protect connector and unit from excess current, Unit can work down to 18V line, with a 10Sec timer once input voltage is lower than 22V.
Detailed Mil-STD-704 is given at table 3.5.1-1 (with restriction per this section above)

Condition	704A	704B	704C	704D	704E	704F
Normal Steady state	Operational					
Abnormal Steady state	Operational [1]					
Emergency Steady state	Operational above 18V [1] / protected below 18V					
Normal Transients	Operational 18V to 50V, 70V optional / protected below 18V	Operational				
Abnormal Transients	Operational 18V to 50V, 80V optional / protected below 18V	Operational above 18V / protected below 18V				
Power Interrupt	Protected / Supports with Holdup unit M4162 (Contact Factory)					
Power Failure	Protected with Auto Recovery					
Reverse Polarity	N/A					Protected

Table 3.5.1.1-1 Operational Range

Note:

1. With timing restrictions under 22V
2. For extended Input Range and working through 16V, 80V & 100V transients or T.H adjustments, please contact factory.

3.5.1.2 Transient Response

Power supply is designed to have a good transient response for input voltage transient.
Output response < 5% for Load transient steps of 60% - 90%.

3.5.1.3 Voltage Distortion

Qualified per Mil-STD-704D LDC103

3.5.1.4 Input Redundancy

M4054 can support parallel operation while fed from two independence power sources.
please note: this configuration does not guarantee output redundancy. Both input source should be active on the same time, otherwise result with over voltage on 3.3VAux (limitation removed on roadmap M4055).

3.5.1.5 Input Voltage Rise Time

There is no limitation on Input voltage rise time, contactor connection is supported.

3.5.1.6 Inrush Currents

Turn-on inrush current can be divided into two categories:
Bus charge Inrush, input current is a function of input voltage rise time, charging the 600µF capacitance.
Outputs Turn-on Inrush, Input current while outputs turn on, typical lower than 1A above the steady state current.

3.5.2 Outputs

3.5.2.1 Outputs Controls: Enable & Inhibit Signals

Outputs are controlled by Enable and Inhibit Signals per VITA 62 definition.
See Table 3.5.2.1-1

INHIBIT*	Low	Low	High	High
ENABLE*	Low	High	Low	High
12V Output	OFF	OFF	ON	OFF
3.3V Aux Output	ON	OFF	ON	OFF

Table 3.5.2.1-1 Outputs Truth table per Signal Status

3.5.2.2 Output Power

Standard configuration will support 12V/64A and 3.3VAux/15A with up to 2mF capacitance on each output.
No Power derating is required for current share application.
Note: for extended output capacitance, please contact factory.

3.5.2.3 Voltage regulation and Ripple

Volage regulation and ripple are measured as sense point location and limits are under all operational range (Line, Load, Temperature). Limit is also given for ACS (12V, 3.3Vaux optional) and 3.3VAux PCS.

Voltage is measured at connector output, Sense line shorted to output.

Statues	12V Output Limits	3.3VAux Output Limits
Single Unit	11.85V – 12.15V	3.28V – 3.42V
Current Share (3.3VAux ACS)	11.85V – 12.15V	3.28V – 3.42V
Current Share (3.3VAux PCS)	11.85V – 12.15V	3.25V – 3.45V

Table 3.5.2.4-1 Outputs Voltage Regulation under all Line, Load and Temperature
Note: limits above are under all Line, Load and Temperature steady state condition

Statues	12V Output Limits	3.3VAux Output Limits
Single Unit	120mV	50mV
Current Share (3.3VAux ACS)	120mV	50mV
Current Share (3.3VAux PCS)	120mV	50mV

Table 3.5.2.4-2 Outputs Voltage Ripple under all Line, Load and Temperature
Notes:

1. limits for 18V-36V Input, under all Loads and Temperature condition
2. Ripple is measured on load after 3-feet harness across 0.1µF capacitor with 10 µF on Load (20MHz BW).

3.5.2.4 Turn-on & Sequencing

Standard configuration 12V rise before 3.3VAux

3.3VAux rise prior to 12V is optional (standard forRoadmap M4055).

3.5.2.5 Sense Connection

Sense lines are provided for 12V and 3.3Vaux outputs for line voltage drop. Each output has its own sense line with a single SENSE RETURN signal. Recommended connection shown on *Figure 3.5.2.5-1*
A8 is 12V Sense lines, B8 is the 3.3Vaux Sense line and D8 is the common-sense return.
Unit sense circuit can compensate up to 0.4V at full load

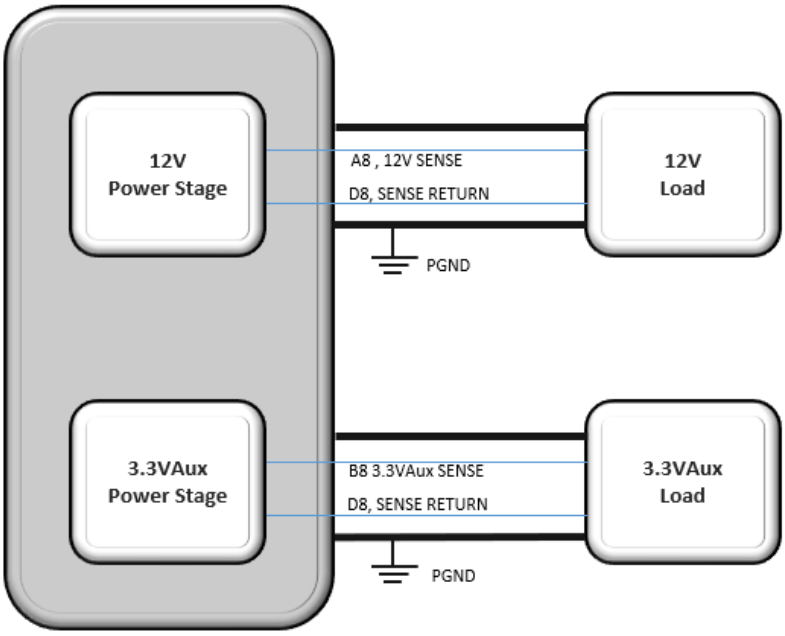


Figure 3.5.2.5-1. Output's sense connection

3.5.2.6 Dynamic Response

Typical performance of 5% output response during a 60% to 90% load dynamic response

3.5.2.7 Current Share

Current share allows the user to connect two or more M4054 units in parallel to double the output power of each rail. No derating is required for current share configuration.
Current share typically provides up to 1-3A balance between unit.
An example of 3 M4054 units, each providing about 50A can be shown on
Figures *3.5.2.7-2*

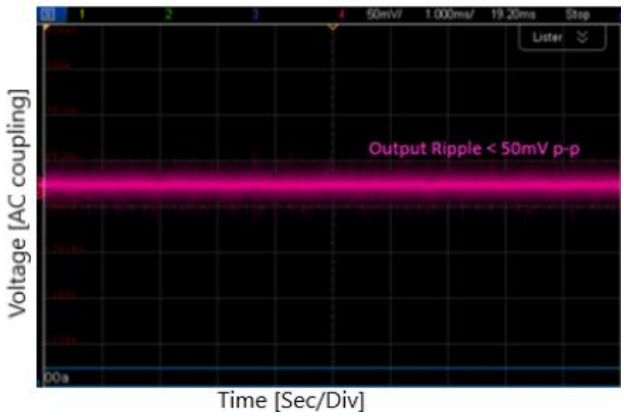


Figure 3.5.2.7-2 (3 units) Output Ripple

12V output is using Active Current Share topology. By comparing the actual current between paralleled units, the unit can provide accurate share balance between outputs with very low susceptibility to power traces and sense connection and no need for voltage drop.
The 3.3Vaux output supports both Passive Current share with voltage drop or ACS with an additional U.D pin.
During a fault condition for both ACS or PCS, both relative outputs will hiccup synchronously to support synchronous turn on into load.
Recommended current share connection is given on *Figure 3.5.2.8-3*

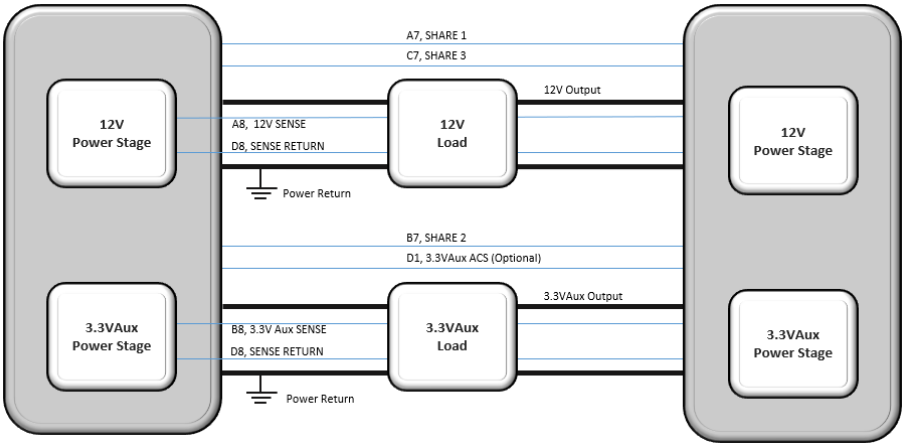


Figure 3.5.2.8-3 current share connection.

Note: For best current share balance, make sure both outputs SENSE lines are connected to a single load point to insure Vout of each outputs is as close as possible to the other.

Please note:

- Current share is an optional configuration
- For 12V output, both A7, C7 need to be connected.
- Typically, current share starts at load above 10% of max load
- No derating is required
- Current share is not a guarantee for redundancy, some failures (E.g. short on output) will result in a failure of both units.
- During Over load condition, both relative outputs will be synchronized with their hiccup to allow Turn-on into full load once the fault condition is removed.
- Multiple current share units are optional.

3.5.2.8 Short Protection

Both 12V and 3.3VAux outputs have an indefinite hiccup for over-Load / short circuit protection. The 3.3Vaux over-load hiccup threshold is 110%-120% of nominal current and 103%-107% for the 12V Output. Output will automatically recover after removal of fault condition.
A short on 3.3VAux rail will not affect the 12V Output, a short on the 12V rail will cause the 3.3VAux to hiccup as well.
While output is at hiccup mode, current during on-time may exceed 140% of max current

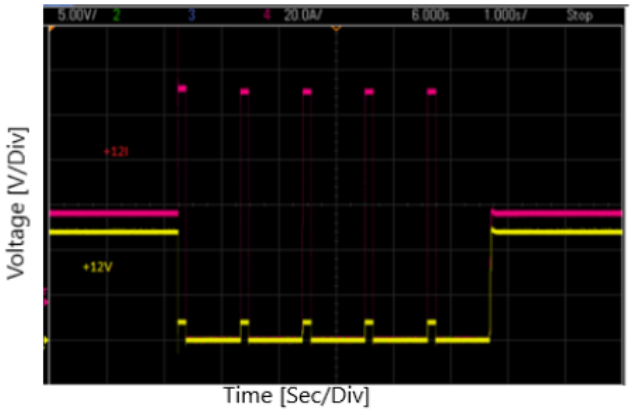


Figure 3.5.2.8-1 Typical 12V Output hiccup and recovery after short

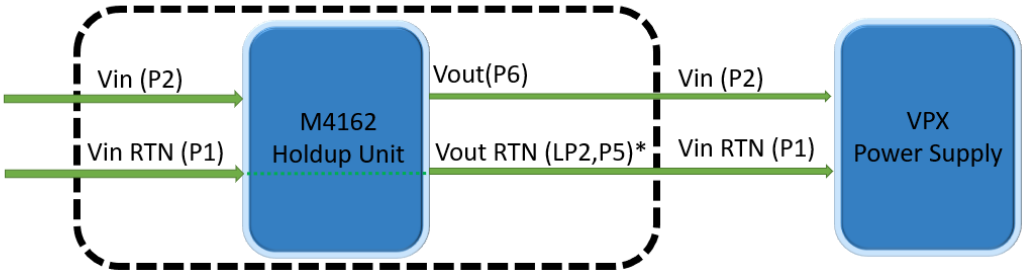
3.5.2.9 Over Voltage Protection

12V output has an active Over Voltage Protection. An O.V condition, caused by internal failure will cause the output to Shut down, with Auto recovery. Off at 13.2-13.6V, on 12.6-12.4V.
3.3VAux Output: 3.9V Output Zener.

3.5.2.10 Hold-up

Requires M4162 unit.

Contact factory for choosing the correct part number.



3.5.3 Signals

3.5.3.1 Fail bit & SYSTEM RESET

Unit has two dedicate Fault signals:
Fail BIT: Indicates that one of the power supply outputs is out of its range, in respect to the expected value depending on Inhibit & Enable status.
Open drain output (Per VITA 65), Normally Open and goes Low during Fail event.
SYSTEM RESET: Indicates that one of the power supply outputs is out of its nominal range.
Open drain output (Per VITA 65), Normally Open and goes Low when output is out of nominal range.
Note: for the M4054 this BIT standard configuration is as “Output”.

3.5.3.2 SYNC IN

Pin can be used to synchronize the power supply switching frequency to an external clock. Standard switching frequency with no Sync In signal applied is 220kHz ±5%. When configured to use Sync, the unit will sync to a signal between 200kHz and 300kHz ±5%. The square wave must be at 3.3V CMOS standard logic levels with a duty cycle between 20% and 80%. The M4054 will sync after 32 cycles within tolerance of external clock. The unit will revert to its internal clock frequency upon any out of specification clock cycles and will need 32 good cycles to resync to the external clock. Contact factory to add Sync_In functionality and to customize its configuration values.

Notes:

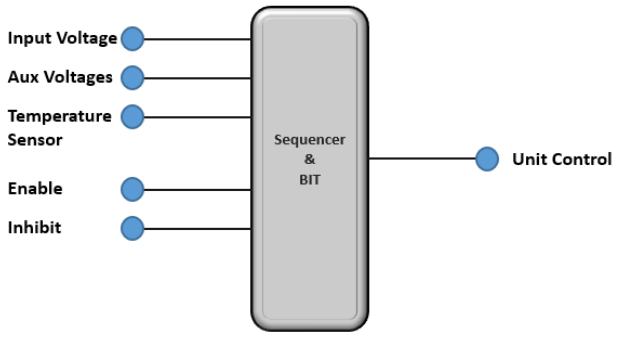
1. Functional is optional, please contact factory.
2. When not used, keep open.
3. Deviating from original frequency may affect efficiency.

3.5.4 Built In Tests

For proper operation, the unit has Built In Test circuit, which continuously monitors Unit's internal functions, such as: Input Voltage, Internal Aux voltage, Temperature, Output voltages and control proper Turn-on and Turn-off Sequence.

Turn on: verification that all parameters are withing proper and all Aux voltage are stabilize before starting outputs Turn-on sequence.

Continues: Monitoring all critical parameters and initiating a controlled Turn-off sequence when required.



3.5.5 Thermal Management

Operational Temperature range is -55°C to +85°C on the surface of the edge that contacts the rack/enclosure. The contacting surface on the rack need to be at lower temperature to account for thermal resistance between the unit and the chassis/cold plate. The M4054 wedge locks are defined as 0.3 °C/W Resistance per Card Edge. The thermal design of the unit will provide a balanced power dissipation between both sides of the unit.
The unit has two thermal sensors.
I2C thermal sensor for 46.11. located at unit hottest spot.
Analog Thermal Sensor for protection and shutdown. Shutdown temperature would be between 90°C to 105°C at unit edge, load depended.
No power derating is required for all operational temperature range

3.5.6 Efficiency

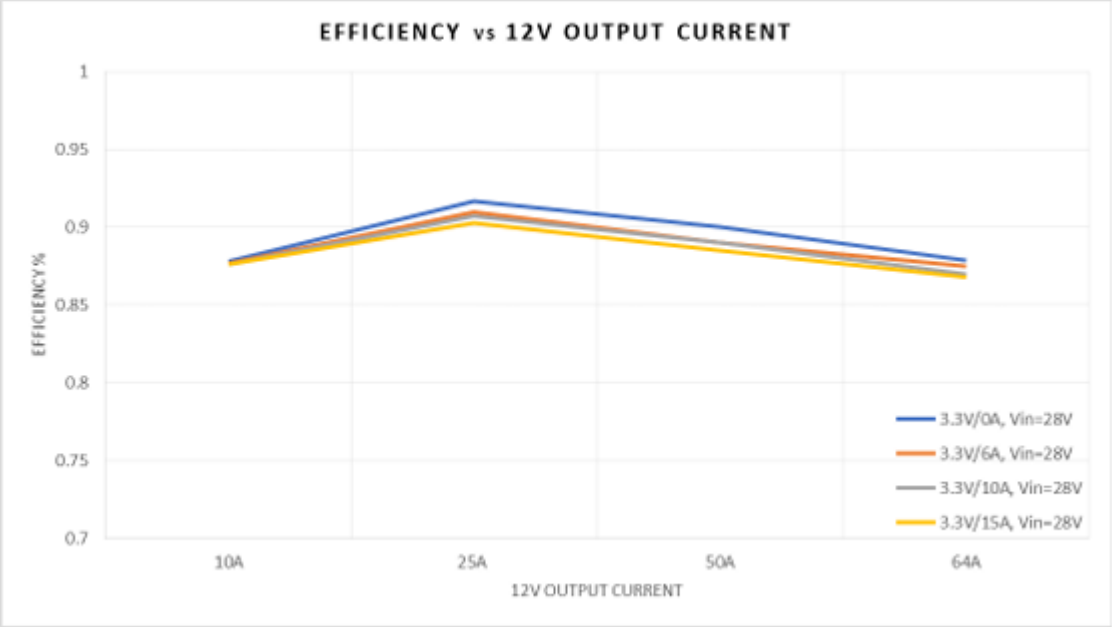
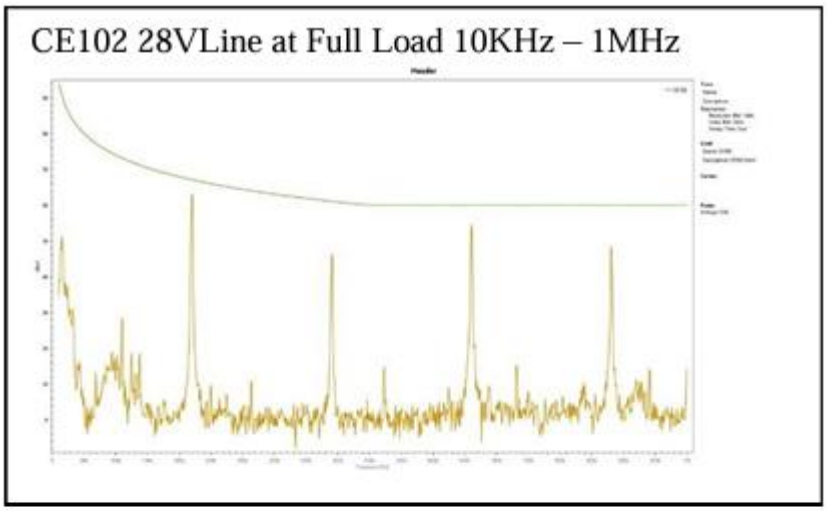


Figure 3.5.6-1. Typical efficiency, room temperature

3.5.7 EMI

EMI Test per Mil-STD-461G for CE102



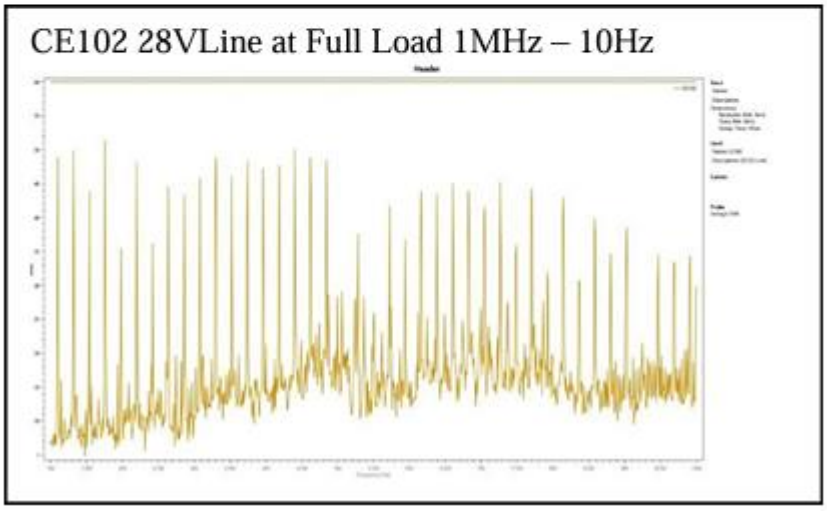


Figure 3.5.7-1. CE102 Full Load, 10KHZ to 150KHZ
Figure 3.5.7-2. CE102 Full Load, 150KHZ to 10MHZ

3.6 System Management

3.6.1 Electrical Interface

Pullups	20KΩ
Capacitance	100PF
Vcc	3.3V
USB-C Port (Roadmap M4055)	Jedec Programing

3.6.2 Communication Protocol

The M4054 can be configured to be one of the two I2C communication protocols: 46.11 Tier 2 IPMC or Advanced I2C protocol.
Slot location, for both options, is defined by VITA62. See table 3.7.2-1.
There following data Sensors are available:
Output Current sensors: Max error of +/-5% or up to +/-1A (the bigger of the two)
Output Voltage sensors: Max error up to +/-0.2V
Input Voltage sensors: Max error up to +/-1.5V
Temperature sensors: ±5C (Internal measurement).

Slot Number	A6	A5	A4	A3	A2/GA2*	A1/GA1*	A0/GA0*	Hardware Address	IPMB
Slot0	0	1	0	0	0 / U	0 / U	0 / U	20	40
Slot1	0	1	0	0	0 / U	0 / U	1 / G	21	42
Slot2	0	1	0	0	0 / U	1 / G	0 / U	22	44
Slot3	0	1	0	0	0 / U	1 / G	1 / G	23	46

Table 3.7.2-1 Address Space
Note: A0÷A6 represent Firmware address and GAx represent the physical Geographical Address.
U = Unconnected; signal is pulled-up on the unit and result as logic "0"
G = Biased to Ground on the Backplane; results in a logical "1"

3.6.2.1 IPMC, 46.11 Tier2

The M4054 design to support both ELMA's ChM and IPMITOOL System Interface. Adjustments can be made to support custom ChM configurations.

Sensor ID	Sensor Type	Name
00	F0h	FRU State Sensor
01	F1h	System IPMB Link Sensor
02	F2h	FRU Health Sensor
03	02h	FRU Voltage Sensor
04	F3h	FRU Temperature Sensor
05	F4h	Payload Test Results Sensor
06	F5h	Payload Test Status Sensor
07	02h	VS1 Voltage
08	03h	VS1 Current
09	02h	3.3VAux Voltage
10	03h	3.3VAux Current
11	01h	Input Voltage
12	02h	Analog Temperature
N/A	N/A	Device Locator Record
N/A	N/A	Device Management

Table 3.6.2.1-1. Sensor Allocation

IPMITOOL Command
SDR List
Sensor List
Fru Print
SEL List
SEL Clear

Table 3.6.2.1-2. Supported *IPMITOOL* Commands

IPMI Command	NetFn	Group ID	CMD
Get Device ID	APP	N/A	01h
Get Self-Test Results	APP	N/A	04h
Get FRU Inventory Area Info	Storage	N/A	10h
Read FRU Data	Storage	N/A	11h
Set Event Receiver	S/E	N/A	00h
Get Event Receiver	S/E	N/A	01h
Get Device SDR info	S/E	N/A	20h
Get Device SDR	S/E	N/A	21h
Reserve Device SDR Repository	S/E	N/A	22h
Get Sensor Reading	S/E	N/A	2Dh
Get VSO Capabilities	Group Extension	VSO (03h)	00h
Set IPMB State	Group Extension	VSO (03h)	09h
Get Device Locator Record ID	Group Extension	VSO (03h)	0Dh
Fru Control Capabilities	Group Extension	VSO (03h)	1Eh
Get FRU Address Info	Group Extension	VSO (03h)	40h

Table 3.6.2.1-3. Supported *RAW IPMI* Commands

Sensor Name	Parameter	Upper Non-Recoverable Threshold	Upper Critical Threshold	Upper Non-Critical Threshold	Lower Non-Critical Threshold	Lower Critical Threshold	Lower Non-Recoverable Threshold
VS1 12V	Voltage	13V	12.8V	12.6V	11.6V	11.4V	11.2V
	Current						
3.3VAux	Voltage	4.2V	4.0V	3.8V	3V	2.8V	2.6V
	Current	24A	22A	20A			
Temperature	Temperature	115°C	110°C	105°C	-55°C	-60°C	-60°C
Vin	Voltage						

Table 3.7.2.1-4. Sensors Thresholds

Note:

1. Thresholds level can be updated, please consult Factory**.**

2. Temperature measurements are taken at unit hottest spot and are load depended.

4. Unit temperature shutdown**,** executed by a sperate sensor in may occur before Upper Non-Recoverable Threshold.

Revision Updates:

Units may have Firmware updates, please refer to specific Dash numbers for firmware updates information.

3.6.2.2 Advanced I2C Protocol

This communication protocol serves as optional when 46.11 compatible ChM is not used. Communication supports read command.

Read Command – 21Hex, deliver 64Bytes of Data.

The communication starts when the master sends a start followed by the unit slave address, command, checksum and a stop. A second start followed by the slave address and a read will be followed by a 64 Bites response.

S	Slave Address	R/W	A	Command	A	Check sum	A	P
	A6:A0	0	0	21 Hex	0	DF Hex	0	

W

S	Slave Address	R/	A	DATA	A	DATA	A	DATA	A	•••	DATA	A	Check sum	N/A	P
	A6:A0	1	0	D7:D0	0	D7:D0	0	D7:D0	0		D7:D0	0	D7:D0	1	

Command – 21Hex read all 64 Bytes
S -Start
P- Stop

Master Transmit	Unit Transmit

Response Byte #	Data Type	Meaning	Interpretation		Reading Range
0	U Integer, MSB First	Echo of Command			21 Hex
1		N/A			00 Hex
2-3	S Integer, MSB First	Temperature -55C to 120C	T(C°)=+/- 7bit Dec		-55°C to 125°C
4-5	U Integer, MSB First	12V VS1 Voltage	V(out) = Data· m2		20.48V
6-7	U Integer, MSB First	3.3V VS2 Voltage	V(out) = Data· m2		20.48V
8-9	U Integer, MSB First	N/A	N/A		N/A
10-11	U Integer, MSB First	N/A	N/A		N/A
12-13	U Integer, MSB First	N/A	N/A		N/A
14-15	U Integer, MSB First	N/A	N/A		N/A
16-17	U Integer, MSB First	12V VS1 Current	V(out) = Data· m3		80A
18-19	U Integer, MSB First	3.3V VS2 Current	V(out) = Data· m3		20A
20-21	U Integer, MSB First	N/A	N/A		N/A
22-23	U Integer, MSB First	N/A	N/A		N/A
24-35	U Integer, MSB First	N/A	N/A		N/A
26-27	U Integer, MSB First	N/A	N/A		N/A
28-29	U Integer, MSB First	Reserved	00Hex		
30-31	U Integer, MSB First	Reserved	00Hex		
32-51	Character String (ASCII)	Part Number	M4054-xxx*	(Note1)	20 Characters
52-53	Decimal, MSB First	Serial Number, 2MSB Dig	X,X Dec	(Note2)	Optional
54-55	Decimal, MSB First	Serial Number, 2LSB Dig	X,X Dec	(Note2)	Optional
56-57	Decimal, MSB First	Date Code	Week, Year	(Note3)	Optional
58-59	Character String (ASCII)	Hardware Rev	B01 & B02 Boards	(Note4)	2 Characters
60-61	Decimal, MSB First	Firmware Rev	X,X,X,X Dec	(Note5)	4 digits
62	U Integer, MSB First	Reserved			AA Hex
63	U Integer, MSB First	Zero Checksum	Value required to make the sum of bytes 0 to 62 added to a multiple of 256		

Note:
M_2 = 20.48/65535
M_3 = 80/65535
M_4 = 20/65535
*Matching unit part number

3.7 Pinout

Pin Number	Pin Name (12V Only)	Function
P1	-DC_IN/ACN	28V Return
P2	+DC_IN/ACL	28V
LP1	CHASSIS	CHASSIS
P3	+12VDC (VS1)	12V Output
P4	POWER_RETURN	Output Return
P5	POWER_RETURN	Output Return
LP2	3.3V_AUX	3.3V Output
P6	+12VDC (VS1)	12V Output
A8	SENSE, +12VDC	12V Sense
B8	SENSE, 3.3V_AUX	3.3V Aux Sense
C8	SENSE, +12VDC	N.C
D8	SENSE_RETURN	Sense Return
A7	SHARE_1	12V Current Share
B7	SHARE_2	3.3V Aux Current Share
C7	SHARE_3	12V ACS
D7	SIGNAL RETURN	Signal Return
A6	SM2	I^2C SCL B
B6	SM3	I^2C SDA B
C6	N Reserved C.	D.N.C.
D6	SYSRESET*	SYSRESET*
A5	GA0*	GA0*
B5	GA1*	GA1*
C5	SM0	I^2C SCL A
D5	SM1	I^2C SDA A
A4	Reserved	D.N.C.
B4	Reserved	D.N.C.
C4	Reserved	D.N.C.
D4	Reserved	D.N.C.
A3	SYNC_IN (UD0)	External Sync Clock
B3	Reserved	N.C.
C3	NED	N.C.
D3	NED RETURN	N.C.
A2	VBAT	D.N.C.
B2	FAIL*	FAIL*
C2	INHIBIT*	INHIBIT*
D2	ENABLE*	ENABLE*
A1	SYNC_OUT (UD1)	N.C.
B1	NVMRO (UD2)	N.C.
C1	GA2* (UD3)	GA2
D1	UD4	3.3V Aux ACS

3.8 Mechanical SCD