

PCI EXPRESS 1.0/2.0/3.0 COPPER/FIBER CONVERSION

PDS - 321

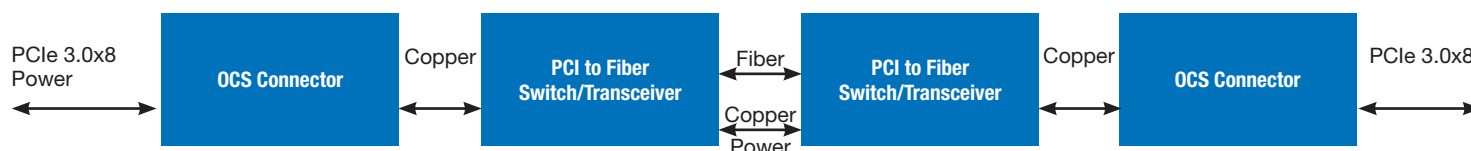


Amphenol's Rugged PCI-Express 1.0/2.0/3.0 fiber optic conversion active assembly provides systems integrators great flexibility as PCI-Express can now be extended over fiber optics in rugged systems. The current product supports a x8 PCI-Express interface on each end of the active cable along with rugged D38999 series 3 receptacles with embedded Oval Contact System high performance contacts for the extension of the interface between sub-systems. The product can support down to PCI-Express 1.0 and up to 3.0 as well as flexibility down to a x1 interface and up to a x8 interface.

FEATURES AND BENEFITS:

- Support for PCI-Express 1.0, 2.0, and 3.0
- I/O expandability from x1 to x8 channel widths
- Power is sourced from the P1 side and then internally routed to the alternate electronics near the P2 connector
- The rugged fiber optic link can be up to 750 meters
- MIL-STD-810 compliant for vibration, temperature, shock, humidity, EMI, etc.
- Integrated with embedded High Speed Oval Contact System contacts for the copper PCI-express interface.
- Max 64Gbps or 8GB/s system throughput for a x8 PCI-express 3.0 link

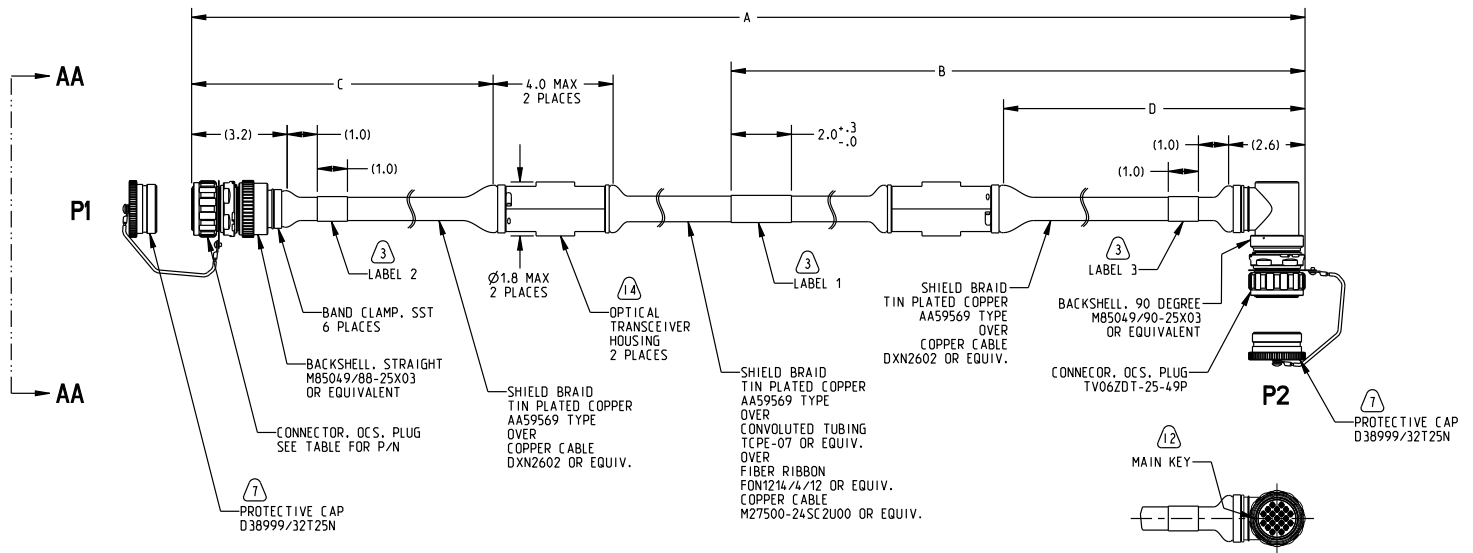
PCI 
EXPRESS®



CF-901201-23X

Customizable Option

- Length Dimensions
- Platings
- Rotations

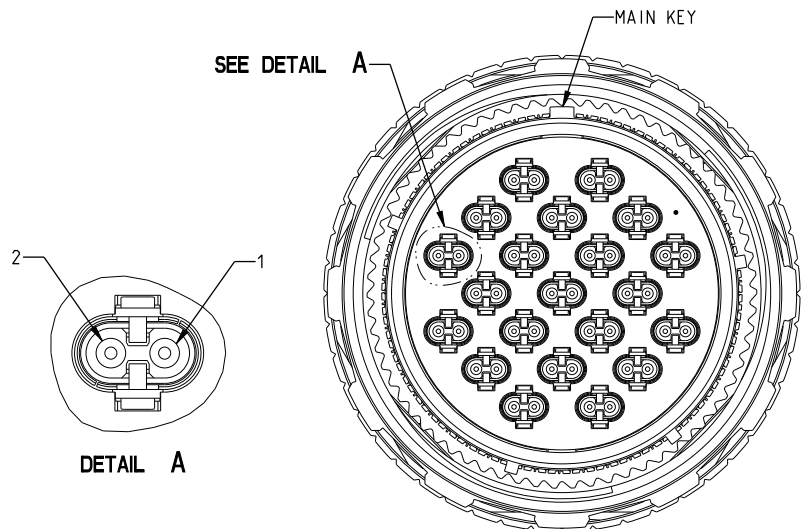


PART NUMBER	A +12.0 -0	B +4.0 -0	C +2.0 0	D +2.0 -0	P1 CONNECTOR	P1 CONN. KEYING
CF-901201-231	248.4	42.5	18.0	11.6	TV06ZDT-25-49P	NORMAL
CF-901201-232	237.9	36.6	17.4	23.8	TV06ZDT-25-49PA	A
CF-901201-233	222.9	27.9	13.7	15.5	TV06ZDT-25-49PB	B
CF-901201-234	245.5	46.7	15.8	16.5	TV06ZDT-25-49PC	C

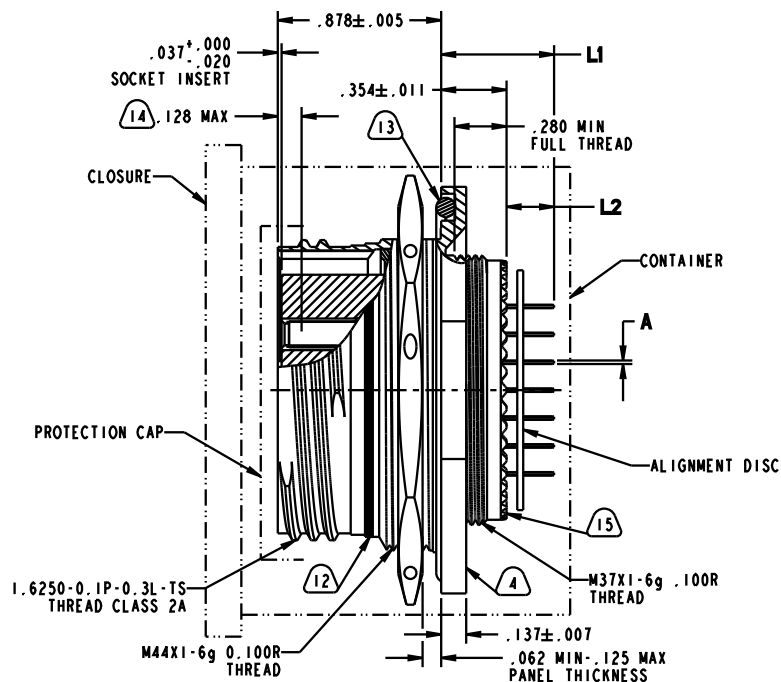
WIRING TABLE

WIRING TABLE		
P1	P2	DESCRIPTION
N1	M1	POS[*]_POS[*]SBC1_PCIE_0_P
N2	M2	POS[*]_POS[*]SBC1_PCIE_0_N
X1	L1	POS[*]_POS[*]SBC1_PCIE_1_P
X2	L2	POS[*]_POS[*]SBC1_PCIE_1_N
Y1	K1	POS[*]_POS[*]SBC1_PCIE_2_P
Y2	K2	POS[*]_POS[*]SBC1_PCIE_2_N
V1	W1	POS[*]_POS[*]SBC1_PCIE_3_P
V2	W2	POS[*]_POS[*]SBC1_PCIE_3_N
U1	J1	POS[*]_POS[*]SBC1_PCIE_4_P
U2	J2	POS[*]_POS[*]SBC1_PCIE_4_N
F1	H1	POS[*]_POS[*]SBC1_PCIE_5_P
F2	H2	POS[*]_POS[*]SBC1_PCIE_5_N
E1	G1	POS[*]_POS[*]SBC1_PCIE_6_P
E2	G2	POS[*]_POS[*]SBC1_PCIE_6_N
T1	D1	POS[*]_POS[*]SBC1_PCIE_7_P
T2	D2	POS[*]_POS[*]SBC1_PCIE_7_N
M1	N1	POS[*]SBC1_POS[*]_PCIE_0_P
M2	N2	POS[*]SBC1_POS[*]_PCIE_0_N
L1	X1	POS[*]SBC1_POS[*]_PCIE_1_P
L2	X2	POS[*]SBC1_POS[*]_PCIE_1_N
K1	Y1	POS[*]SBC1_POS[*]_PCIE_2_P
K2	Y2	POS[*]SBC1_POS[*]_PCIE_2_N
W1	V1	POS[*]SBC1_POS[*]_PCIE_3_P
W2	V2	POS[*]SBC1_POS[*]_PCIE_3_N
J1	U1	POS[*]SBC1_POS[*]_PCIE_4_P
J2	U2	POS[*]SBC1_POS[*]_PCIE_4_N
H1	F1	POS[*]SBC1_POS[*]_PCIE_5_P
H2	F2	POS[*]SBC1_POS[*]_PCIE_5_N
G1	E1	POS[*]SBC1_POS[*]_PCIE_6_P
G2	E2	POS[*]SBC1_POS[*]_PCIE_6_N
D1	T1	POS[*]SBC1_POS[*]_PCIE_7_P
D2	T2	POS[*]SBC1_POS[*]_PCIE_7_N

WIRING TABLE		
P1	P2	DESCRIPTION
B1	--	POS_[*]_PCIE_12VDC_PWR
B2	--	POS_[*]_PCIE_12VDC_PWR_RTN
C1	--	POS_[*]_PCIE_12VDC_PWR
C2	--	POS_[*]_PCIE_12VDC_PWR_RTN
A1	--	RESERVED_NC
A2	--	RESERVED_NC
P1	--	RESERVED_NC
P2	--	RESERVED_NC
R1	--	RESERVED_NC
R2	--	RESERVED_NC
--	A1	RESERVED_NC
--	A2	RESERVED_NC
--	B1	RESERVED_NC
--	B2	RESERVED_NC
--	C1	RESERVED_NC
--	C2	RESERVED_NC
--	P1	RESERVED_NC
--	P2	RESERVED_NC
--	R1	RESERVED_NC
--	R2	RESERVED_NC



Amphenol
Aerospace



SEE DETAIL B

INNER TAILS

OUTER TAILS

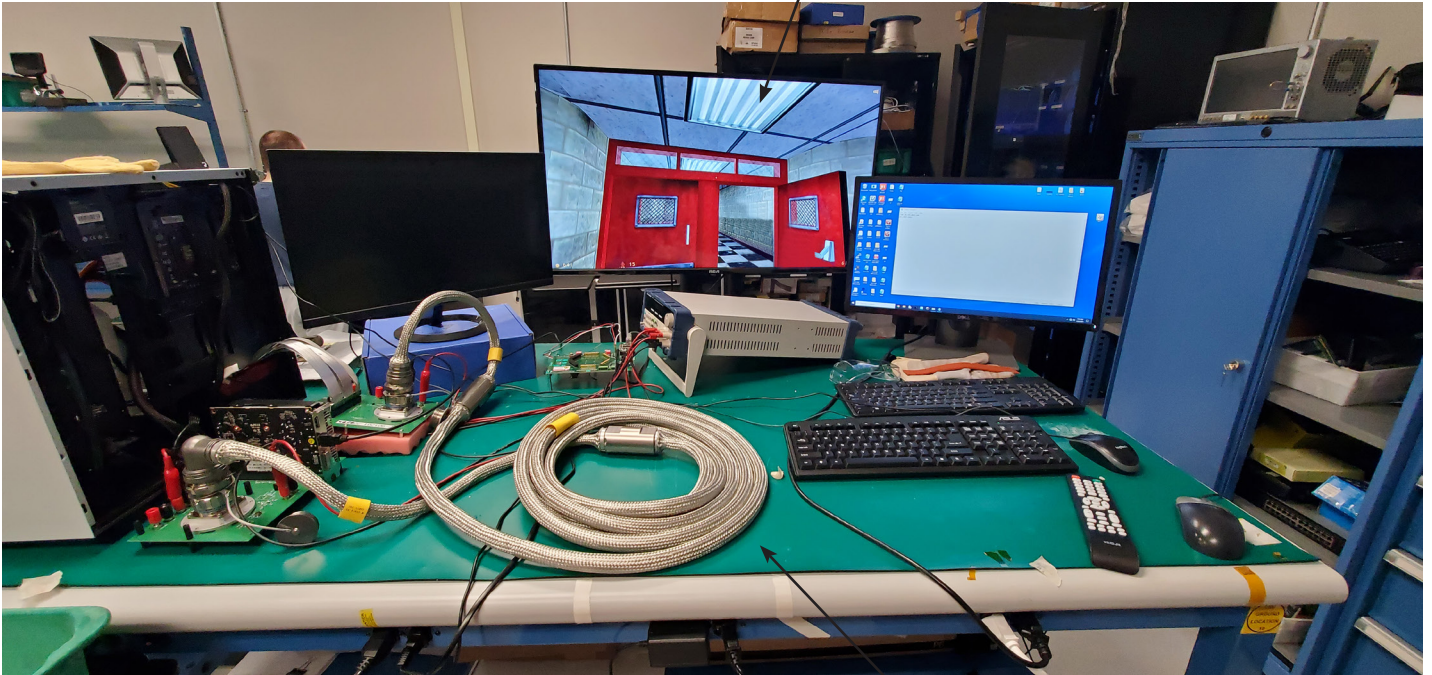
DETAIL B

The drawing consists of two parts. The top part is a plan view of a circular object with an octagonal outer boundary. Inside, there is a circular area containing a 4x4 grid of 16 small, rounded rectangular features, each with two internal circular elements. A leader line points from the text 'SEE DETAIL B' to one of these features. The bottom part is a detailed cross-sectional view of one of these features, showing an oval shape with two circular elements at the bottom. Leader lines point from the text 'INNER TAILS' to the top edges and 'OUTER TAILS' to the bottom edges of the oval. The text 'DETAIL B' is centered below this view.

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TESTING

Graphics over PCIe 3.0x8 Fiber



Product Under Test