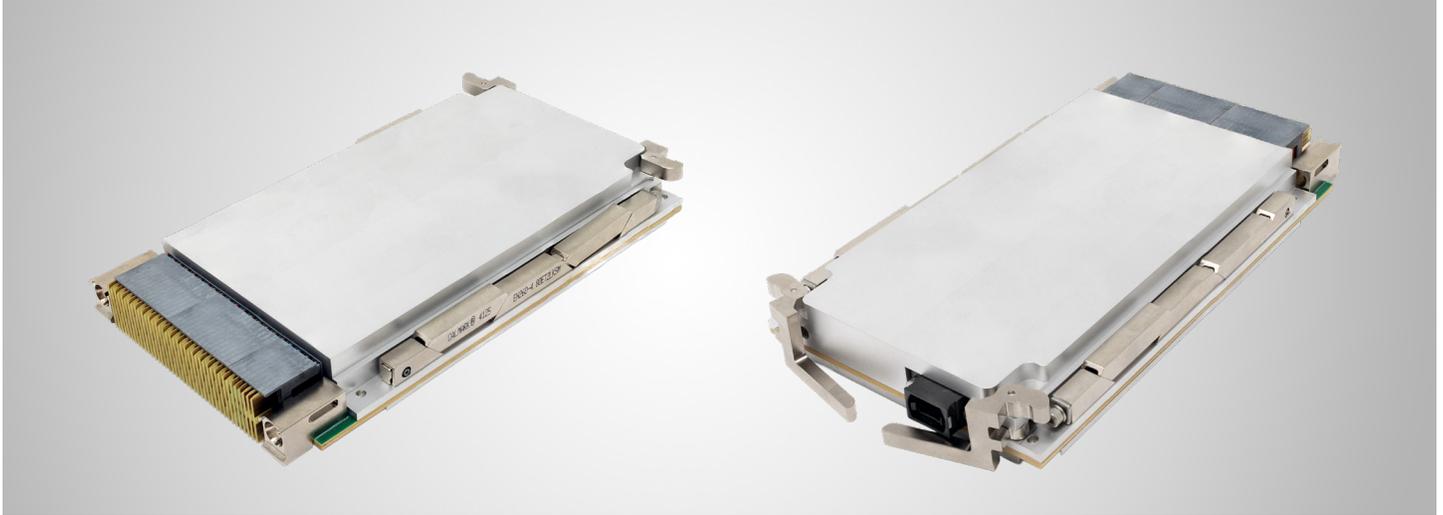


SOSA-ALIGNED 3U R-VPX HIGH SPEED ETHERNET SWITCH

ENABLED WITH 10G/25G TSN MACSEC PROTOCOLS

PDS - 380



36-Channel Switch that Conforms to SLT3-SWH-6F1U7U-14.4.14 and MOD3-SWH-6F1U7U-16.4.15-2 Slot Profiles.

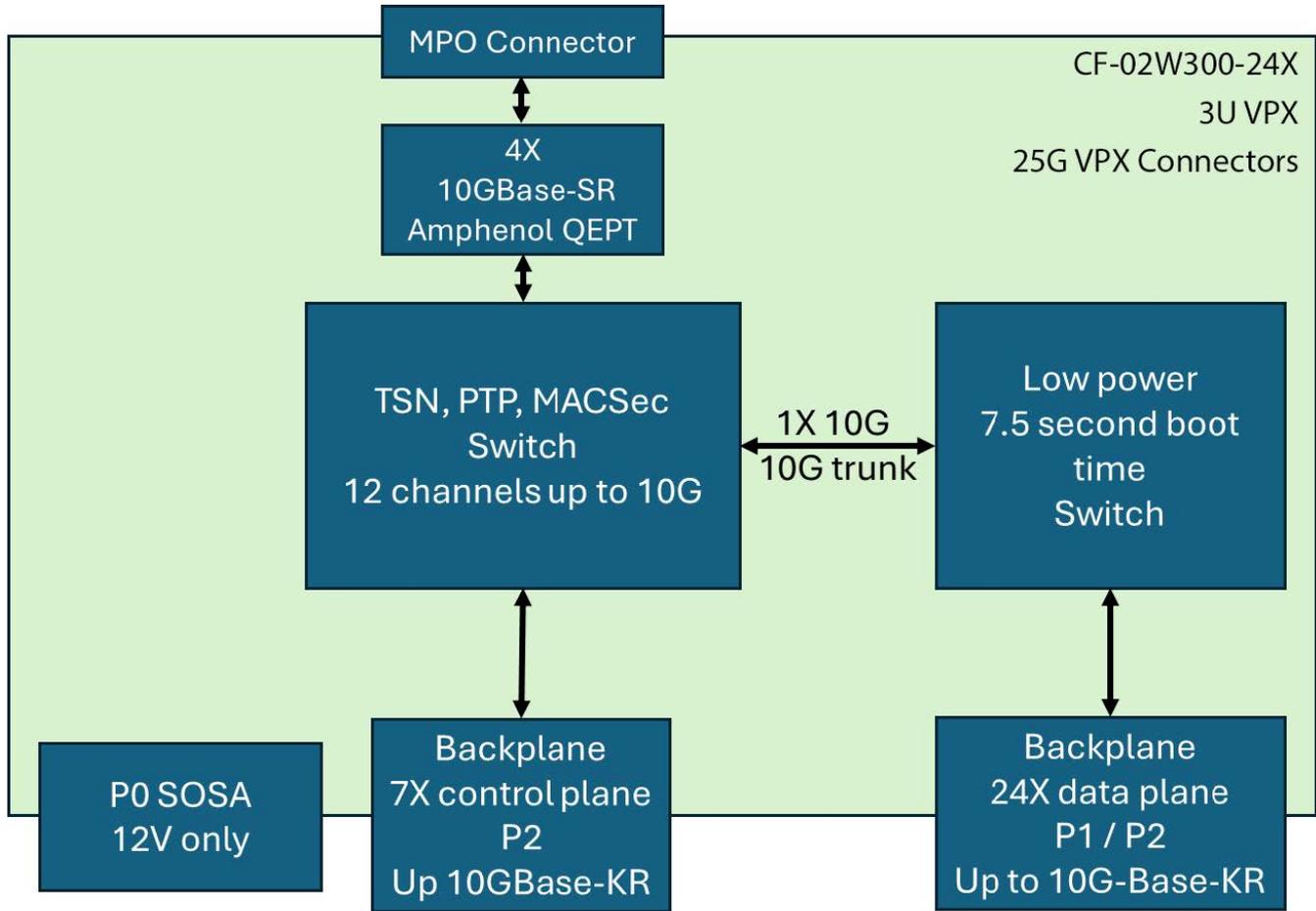
Amphenol's 36-Channel 1G/10G/25G copper and fiber optic Ethernet switch in 3U VPX SOSA-aligned form factor conforms to SLT3-SWH-6F1U7U-14.4.14 and MOD3-SWH-6F1U7U-16.4.15-2 slot profiles. The switch consists of a TSN and MACSec enabled 12-channel Ethernet switch for the seven control plane ports, four fiber optic ports, and a trunk port to the data plane switched devices. The data plane switched devices have access to the entire Ethernet mesh through a low power, less managed, and short boot-time 10G Ethernet switch ASIC.

FEATURES & BENEFITS:

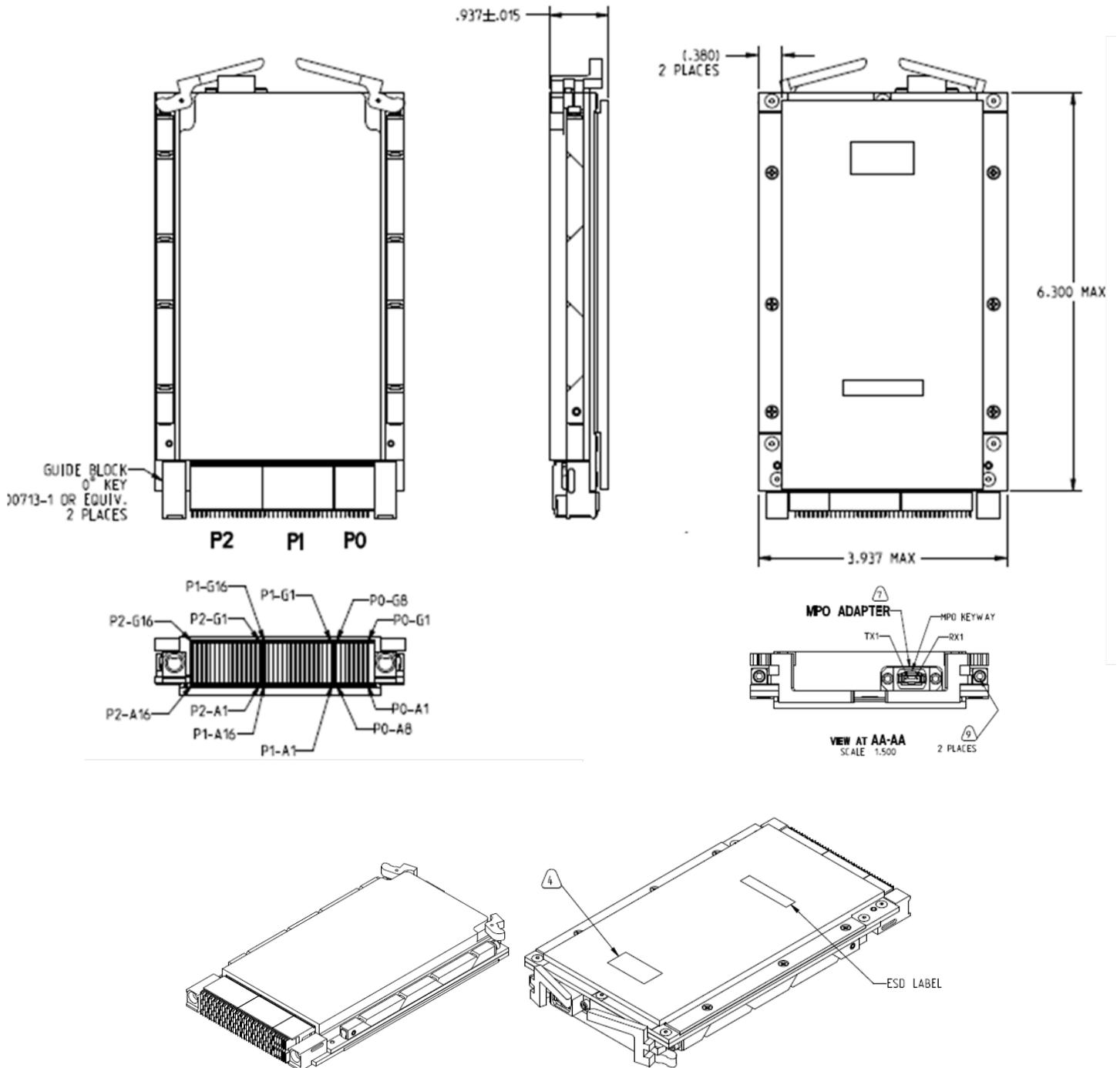
- 36-Channel Support: Seven control plane channels at up to 10GBase-KR and four channels of up to 10GBase-SR with fill acceleration for TSN/MACSec functions. 24 channels of data plane switching up to 10GBase-SR.
- Multimode Fiber Compatibility: Designed for OM3/OM4/OM5 multimode fiber systems typically used in data center environments through rugged MTP connector.
- SOSA-aligned slot profile: for 24 channels of data plane devices and 7 channels of control plane devices.
- Low power and rugged operation: Designed for -40-+85C operation in rugged military environments at high altitudes. Typical power consumption at 50 watts or less.
- Designed for Industry 4.0 and IoT.

Part Number	Description
CF-02W300-24X	Switch – Conduction Cooled

BLOCK DIAGRAM



DIMENSIONAL INFORMATION



P0 I/O CHART							
	G	F	E	D	C	B	A
1	+12V	+12V	+12V	NC	NC	NC	NC
2	+12V	+12V	+12V	NC	NC	NC	NC
3	NC	NC	NC	NC	NC	NC	NC
4	ISCL2	ISDA2	GND	NC	GND	BPRSETn	NVMRO
5	GAP	GA4	GND	NC	GND	ISCL1	ISDA1
6	GA3	GA2	GND	NC	GND	GA1	GA0
7	TCK	GND	TDO	TDI	GND	TMS	NC
8	GND	NC	NC	GND	NC	NC	GND

MPO ADAPTER I/O CHART	
ID	SIGNAL
RX1	25G-SR_RX1
RX2	25G-SR_RX2
RX3	25G-SR_RX3
RX4	25G-SR_RX4
TX4	25G-SR_TX4
TX3	25G-SR_TX3
TX2	25G-SR_TX2
TX1	25G-SR_TX1

P1 I/O CHART								
		G	F	E	D	C	B	A
1	DATA PLANE STACKING PORT 1	GDiscrete1	GND	P1_10G-KR_TX#	P1_10G-KR_TX	GND	P1_10G-KR_RX#	P1_10G-KR_RX
		GND	P2_10G-KR_TX#	P2_10G-KR_TX	GND	P2_10G-KR_RX#	P2_10G-KR_RX	GND
		P1-VBAT	GND	P3_10G-KR_TX#	P3_10G-KR_TX	GND	P3_10G-KR_RX#	P3_10G-KR_RX
		GND	P4_10G-KR_TX#	P4_10G-KR_TX	GND	P4_10G-KR_RX#	P4_10G-KR_RX	GND
2	DATA PLANE PORT 1	SYS_CON#	GND	P5_10G-KR_TX#	P5_10G-KR_TX	GND	P5_10G-KR_RX#	P5_10G-KR_RX
		GND	P6_10G-KR_TX#	P6_10G-KR_TX	GND	P6_10G-KR_RX#	P6_10G-KR_RX	GND
		Reserved	GND	P7_10G-KR_TX#	P7_10G-KR_TX	GND	P7_10G-KR_RX#	P7_10G-KR_RX
		GND	P8_10G-KR_TX#	P8_10G-KR_TX	GND	P8_10G-KR_RX#	P8_10G-KR_RX	GND
3	DATA PLANE PORT 2	MP01-TD	GND	P9_10G-KR_TX#	P9_10G-KR_TX	GND	P9_10G-KR_RX#	P9_10G-KR_RX
		GND	P10_10G-KR_TX#	P10_10G-KR_TX	GND	P10_10G-KR_RX#	P10_10G-KR_RX	GND
		MP01-RD	GND	P11_10G-KR_TX#	P11_10G-KR_TX	GND	P11_10G-KR_RX#	P11_10G-KR_RX
		GND	P12_10G-KR_TX#	P12_10G-KR_TX	GND	P12_10G-KR_RX#	P12_10G-KR_RX	GND
4	DATA PLANE PORT 3	Reserved	GND	P13_10G-KR_TX#	P13_10G-KR_TX	GND	P13_10G-KR_RX#	P13_10G-KR_RX
		GND	P14_10G-KR_TX#	P14_10G-KR_TX	GND	P14_10G-KR_RX#	P14_10G-KR_RX	GND
		MaskableRST*	GND	P15_10G-KR_TX#	P15_10G-KR_TX	GND	P15_10G-KR_RX#	P15_10G-KR_RX
		GND	P16_10G-KR_TX#	P16_10G-KR_TX	GND	P16_10G-KR_RX#	P16_10G-KR_RX	GND

P2 I/O CHART								
		G	F	E	D	C	B	A
1	DATA PLANE STACKING PORT 4	Reserved	GND	P17_10G-KR_TX#	P17_10G-KR_TX	GND	P17_10G-KR_RX#	P17_10G-KR_RX
		GND	P18_10G-KR_TX#	P18_10G-KR_TX	GND	P18_10G-KR_RX#	P18_10G-KR_RX	GND
		Reserved	GND	P19_10G-KR_TX#	P19_10G-KR_TX	GND	P19_10G-KR_RX#	P19_10G-KR_RX
		GND	P20_10G-KR_TX#	P20_10G-KR_TX	GND	P20_10G-KR_RX#	P20_10G-KR_RX	GND
2	DATA PLANE PORT 5	Reserved	GND	P21_10G-KR_TX#	P21_10G-KR_TX	GND	P21_10G-KR_RX#	P21_10G-KR_RX
		GND	P22_10G-KR_TX#	P22_10G-KR_TX	GND	P22_10G-KR_RX#	P22_10G-KR_RX	GND
		Reserved	GND	P23_10G-KR_TX#	P23_10G-KR_TX	GND	P23_10G-KR_RX#	P23_10G-KR_RX
		GND	P24_10G-KR_TX#	P24_10G-KR_TX	GND	P24_10G-KR_RX#	P24_10G-KR_RX	GND
3	CONTROL PLANE ONE OF WHICH IS STACKING	GND	GND	GND	GND	GND	GND	GND
		GND	CS01_10G-KR_TX#	CS01_10G-KR_TX	GND	CS01_10G-KR_RX#	CS01_10G-KR_RX	GND
		MP02-TD	GND	CP04_10G-KR_TX#	CP04_10G-KR_TX	GND	CP04_10G-KR_RX#	CP04_10G-KR_RX
		GND	CP03_10G-KR_TX#	CP03_10G-KR_TX	GND	CP03_10G-KR_RX#	CP03_10G-KR_RX	GND
4	CONTROL PLANE ONE OF WHICH IS STACKING	MP02-RD	GND	CP02_10G-KR_TX#	CP02_10G-KR_TX	GND	CP02_10G-KR_RX#	CP02_10G-KR_RX
		GND	CP01_10G-KR_TX#	CP01_10G-KR_TX	GND	CP01_10G-KR_RX#	CP01_10G-KR_RX	GND
		NC	GND	CP06_10G-KR_TX#	CP06_10G-KR_TX	GND	CP06_10G-KR_RX#	CP06_10G-KR_RX
		GND	CP05_10G-KR_TX#	CP05_10G-KR_TX	GND	CP05_10G-KR_RX#	CP05_10G-KR_RX	GND

SOFTWARE – Control Plane Side - ~50 second boot

Manuals available upon request

Based on a new generation of highly integrated packet processors, this module is designed to deliver a full portfolio of scalable, high-performance, low-power, small-footprint, feature-rich Ethernet switch modules, optimized for industrial and Internet of Things (IoT) applications operating in extended temperature range. The extensive support in Time-Sensitive Networking (TSN) IEEE standards and High-availability Seamless Redundancy (HSR/PRP), empowers the transition to real-time communication solutions.

Offering these standards in a single chip guarantees end-to-end transmission of high-priority traffic with deterministic latency and increased reliability. Ironman integration of groundbreaking technologies TIPS (Telemetry, Intelligence, Performance, Security) technology lays out the essential foundation for innovations in network visibility, intelligence, performance, and security. Intelligent workload management provides optimized data processing at or near the network access edge, reducing hybrid cloud bandwidth requirements; insightful telemetry reinforces automation and expedites forensic analytics; advanced security features underpin trustworthiness and provide network embedded protection from ever evolving security threats. Integrates forwarding tables, Longest Prefix Match (LPM) tables, and flexible multiple TCAM lookups, designed to address Industrial Access deployment needs. With comprehensive embedded security services include high-bandwidth IEEE 802.1AE Media Access Control Security (MACsec) Engine, at full device bandwidth processing capacity can provide cryptography-based security for Ethernet traffic. The family also supports device level security including Secured Boot and Secured Storage. The module Integrates Dual-Core ARM-v8.2 Cortex-A55 high-performance CPU Cluster, designed to meet requirements of modern Network Operation Systems. Additionally, the module integrates multiple ARMv7 Cortex-M3 (CM3) uControllers, each with its own memory that can be used running control functions such as PoE Stack, Device Initialization, Telemetry Collection or User-Specific processes and tasks. The Control and Management subsystem integrates a 16-bit DDR4 memory controller and supports rich interfaces for the internal and external management functions, that include PCI Express (PCIe) Gen3.0, Ethernet Port, eMMC, QSPI-Flash, NAND-Flash, USB 2.0 and others.

Furthermore, the module allows a wide-range modern packet processing feature-set, based on Marvell® extended-bridging (eBridge) architecture; virtual overlay networking with programmable tunnel header encapsulation; real-time flow granular telemetry and observability capabilities to facilitate network adaptation; robust QoS, load-balancing schemes and advanced congestion mechanisms, designed to meet the modern networks' needs. The device is compatible with the Marvell Prestera® DX Family software to enable a rapid product development and time-to market.

Network Features

- Jumbo Frames support
- Cut-through operation to minimize traffic latency
- IEC 62439-3 - HSR/PRP High available seamless redundancy (Parallel Redundancy Protocol)
- Time-Sensitive Networking (TSN) IEEE
- Parallel (x8) and Serial LED interface for port activity status
- Highly scalable (cascade up to 1K modules)

Memory, Security, and Hardware Features

- High bandwidth DDR4 (1G/2G options)
- eMMC (up to 256G)
- PCIe Gen3 dev
- Trusted / secure boot support

- IEEE 802.3ae standard compliant MACsec engine with capacity to process, encrypt, and decrypt the entire devices bandwidth bi-directional traffic

Industrial Features

- G.8032, ERPS Ring Protection
- High accuracy one and two-step PTP compliant with IEEE 1588v1/v2 and ITU-T G.8273.2 Class C with IEEE 802.1AS02020 support
- SyncE compliant
- IEC 62439-3 – HSR/PRP high available seamless redundancy (Parallel Redundancy Protocol)

TSN

- IEEE 802.1CM-2018 profile B
- IEEE 802.1AS-2020 – timing synchronization with 4 time domains plus 1 free running clock
- IEEE 802.1Qav, IEEE 802.1Qbv, IEEE 802.1Qbu and 802.3br, IEEE 802.1Qci, IEEE 802.1CB

Many more features and manual available on request.

Stacking	Configuring VLANs	Configuring IGMP Snooping
Stacking Ring Topology	Defining VLAN Properties	Configuring MLD Snooping
Stacking Chain Topology	Defining VLAN Membership	Viewing IGMP/MLD IP Multicast Groups
Stacking Members and Unit ID	Defining VLAN Interface Settings	Defining Multicast Router Ports
Removing and Replacing Stacking Member	Configuring GARP	Defining Forward All Multicast
Exchanging Stacking Members	Defining GARP	Defining Unregistered Multicast Settings
Switching the Stacking Master	Defining GVRP	Managing System Files
Configuring System Time	Viewing GVRP Statistics	Downloading System Files
Configuring Daylight Savings Time	Defining IP Addresses	Firmware Download
Configuring SNTP	Configuring IP Addressing	Configuration Download
Polling for Unicast Time Information	Defining IP Addresses	Uploading System Files
Polling for Anycast Time Information	Defining ARP	Upload Type
Broadcast Time Information	Defining Domain Name Servers	Software Image Upload
Defining SNTP Settings	Defining DNS Servers	Configuration Upload
Configuring Device Security	Defining DNS Host Mapping	Copying Files
Configuring Management Security	Defining the Forwarding Database	Restoring the Default Configuration File
Configuring Authentication Methods	Defining Static Forwarding Database Entries	Configuring Quality of Service
Defining Access Profiles	Defining Dynamic Forwarding Database Entries	Quality of Service Overview
Defining Profile Rules	Configuring Spanning Tree	VPT Classification Information
Defining Authentication Profiles	Defining Classic Spanning Tree	CoS Services
Mapping Authentication Methods	Defining STP on Interfaces	Defining General QoS Settings
Defining RADIUS Settings	Defining Rapid Spanning Tree	Configuring QoS General Settings
Defining TACACS+ Authentication	Defining Multiple Spanning Tree	Restoring Factory Default QoS Interface Settings
Configuring Passwords	Defining MSTP Instance Settings	Defining Queues
Defining Local Users	Defining MSTP Interface Settings	Defining Bandwidth Settings
Defining Line Passwords	Configuring SNMP	Mapping CoS Values to Queues
Defining Enable Passwords	SNMP v1 and v2c	Mapping DSCP Values to Queues
Configuring Network Security	SNMP v3	Defining QoS Basic Mode
Network Security Overview	Configuring SNMP Security	Defining Basic Mode Settings
Port-Based Authentication	Defining SNMP Security	Rewriting Basic Mode DSCP Values
Advanced Port-Based Authentication	Defining SNMP View	Defining QoS Advanced Mode
Defining Port Authentication Properties	Defining SNMP Group Profiles	Setting Policy Binding
Defining Port Authentication	Defining SNMP Group Members	Managing Device Diagnostics
Configuring Multiple Hosts	Defining SNMP Communities	Configuring Port Mirroring
Defining Authentication Hosts	SNMP Communities Basic Table	Viewing Statistics
Viewing EAP Statistics	SNMP Communities Advanced Table	Viewing Interface Statistics
Defining Access Control Lists	Configuring SNMP Notifications	Viewing Interface Statistics
Defining IP Based Access Control Lists	Defining SNMP Notification Global Parameters	Receive Statistics
Defining MAC Based Access Control Lists	Defining SNMP Notification Filters	Transmit Statistics
Binding Device Security ACLs	Defining SNMP Notification Recipients	Viewing Etherlike Statistics
Managing Port Security	SNMPv1,2c Notification Recipients	Managing RMON Statistics
Enabling Storm Control	SNMPv3 Notification Recipients	Viewing RMON Statistics
Configuring System Logs	Configuring Multicast Forwarding	Configuring RMON History
Defining General Log Properties	Multicast Forwarding	Defining RMON History Control
Viewing Memory Logs	Typical Multicast Setup	Viewing the RMON History Table
Viewing Flash Logs	Multicast Operation	Configuring RMON Events
Defining System Log Servers	Multicast Registration	Defining RMON Events Control
Configuring Interfaces	Multicast Address Properties	Viewing the RMON Events Logs
Configuring Ports	Defining Multicast Properties	Defining RMON Alarms
Aggregating Ports	Adding MAC Group Address	
Configuring LACP	Adding IP Multicast Groups	

SOFTWARE – Data Plane Side – ~10 second boot

Manuals available upon request

CLI and Web Interface

IPV4 / IPV6 routing

Information on links and routing

Tagged and untagged VLAN configurations

Trunk Link Aggregation

Port Mirroring

Port Based QoS

802.1P QoS

Rate Limitations

Loop Detection

Multicast IGMP Snooping

Cable Diagnostics

Amphenol Ruggedization Design

Overview

Amphenol integrated electronic products are designed and manufactured to our Ruggedization guidelines listed below. These guidelines ensure years of reliable operation in harsh environment applications where extreme operating temperatures, shock, vibration, and corrosive atmospheres are regularly experienced. Unless otherwise noted, the parts conform to the below specifications.

Temperature:

- Operating Temperature - thermal cycles between -40°C and 85°C while device is operating.
- Temperature is measured at chassis housing or card edge
- Storage temperature - thermal cycles between -55°C and 125°C

Humidity

- Operating Humidity - humidity cycle between 0-100% non-condensing humidity while device operating
- Storage Humidity - humidity cycle between 0-100% condensing humidity

Sealing

- Sealing can be optionally provided at the MIL-DTL-38999 interface with up to 10-5 cc/sec performance

Shock and Vibration

- Sine Vibration - 10g Peak. 5-2,000Hz
 - Based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 5 to 44 Hz, depending on specific test.
- Random Vibration - 0.0005 @ 5Hz, 0.1 @ 15 Hz, 0.1 @ 2,000 Hz
 - 60 minutes per axis, in each of three mutually perpendicular axes.
- 40 G Peak Shock Cycle
 - Three hits in each axis, both directions, 1/2 sine and terminal-leak saw tooth, total 36 hits

Fluid Susceptability

- MIL-DTL-38999 receptacle interface per EIA-364-10E

Altitude:

- -1,500 to 60,000 ft Altitude Testing w/ Rapid Depressurization

Electromagnetic Compatibility

- Designed to comply with MIL-STL-461E

Printed Circuit Board Assemblies

- Conformal Coat
- Amphenol performs Conformal Coating to both sides of printed circuit board assemblies using HUSMISEAL IB31 in accordance with IPC-610, Class 3.
- Printed Circuit Board Rigidity
- Amphenol printed circuit boards are fabricated in accordance with IPC-6012, Class 3
- Printed Circuit Board Fabrication
- Amphenol printed circuit boards acceptance criteria is in accordance with IPC-610, Class 3.

Reliability Predictions (MTBF)

Amphenol can perform Mean Time Between Failure (MTBF) reliability analysis in full compliance with MIL-HDBK-217F-1 Parts Count Prediction and MIL-HDBK-217F-1 Parts Stress Analysis Prediction. We can also perform reliability analyses in full compliance of ANSI/VITA 51.1 if it is required or preferred over the later method

Notice: Specifications are subject to change without notice. Contact your nearest Amphenol Corporation Sales Office for the latest specifications. All statements, information and data given herein are believed to be accurate and reliable but are presented without guarantee, warranty, or responsibility of any kind, expressed or implied. Statements or suggestions concerning possible use of our products are made without representation or warranty that any such use is free of patent infringement and are not recommendations to infringe any patent. The user should assume that all safety measures are indicated or that other measures may not be required. Specifications are typical and may not apply to all connectors.

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