Amphenol Aerospace

CF-020011-01X

Thermal Analysis

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Electronic Cooling Solutions Inc.

Contents

Objectives

1. To determine that the critical components on the CF-020011-01X board are within their thermal limits:

   a) **70°C at sea level**

   b) **-10°C at sea level**

   c) **85°C at sea level**

   d) **-40°C at sea level**

   At 3 different power levels:

   a) **SNC Op.** – Total Power of 74.72W

   b) **10G Op**. - Total Power of 84.62W

   c) **Worst Case** – Total Power of 115.6W

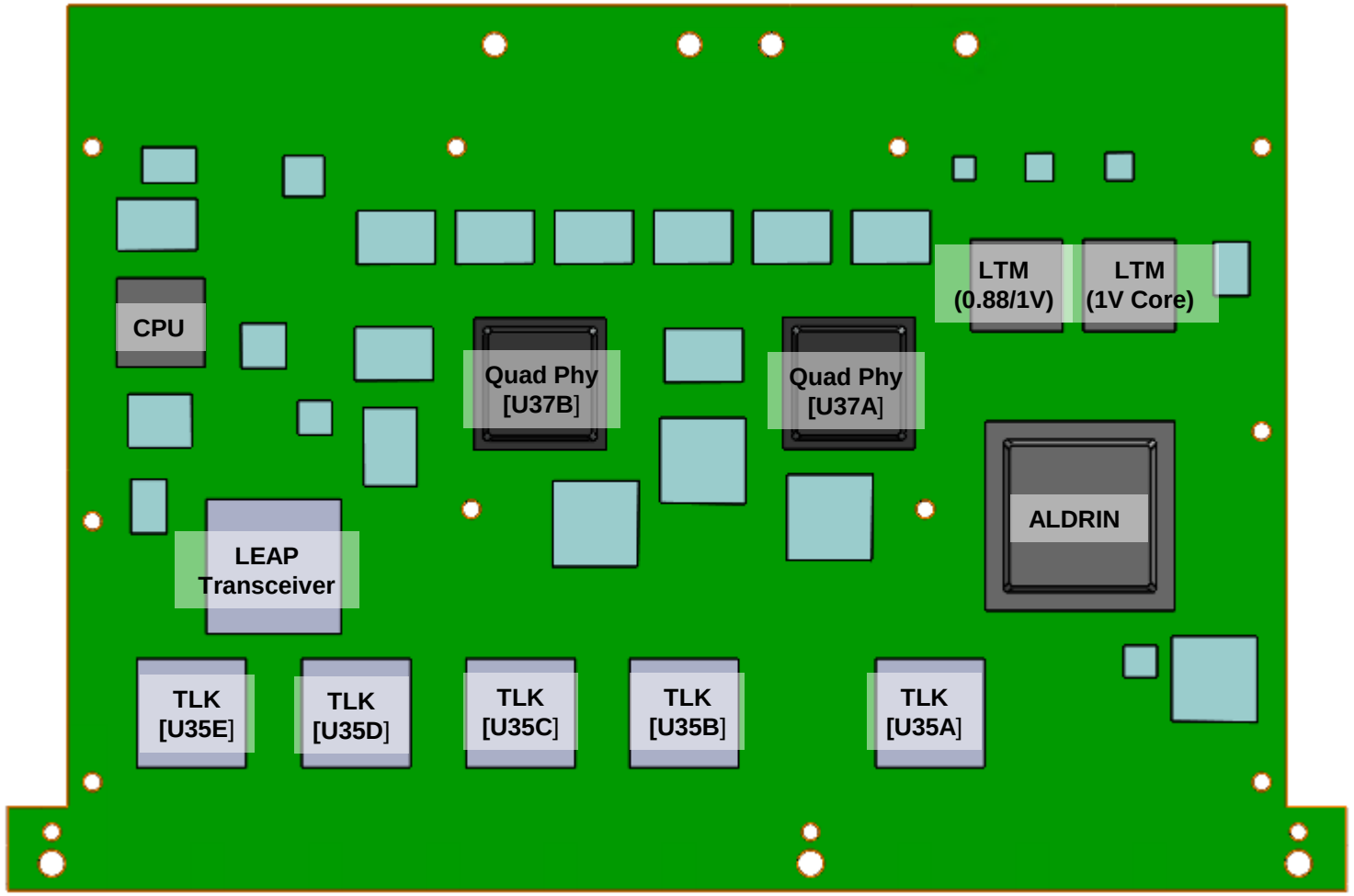
2. To determine the temperature of the cold plate to keep all the ICs within operating limits within the specified environments.

Approach

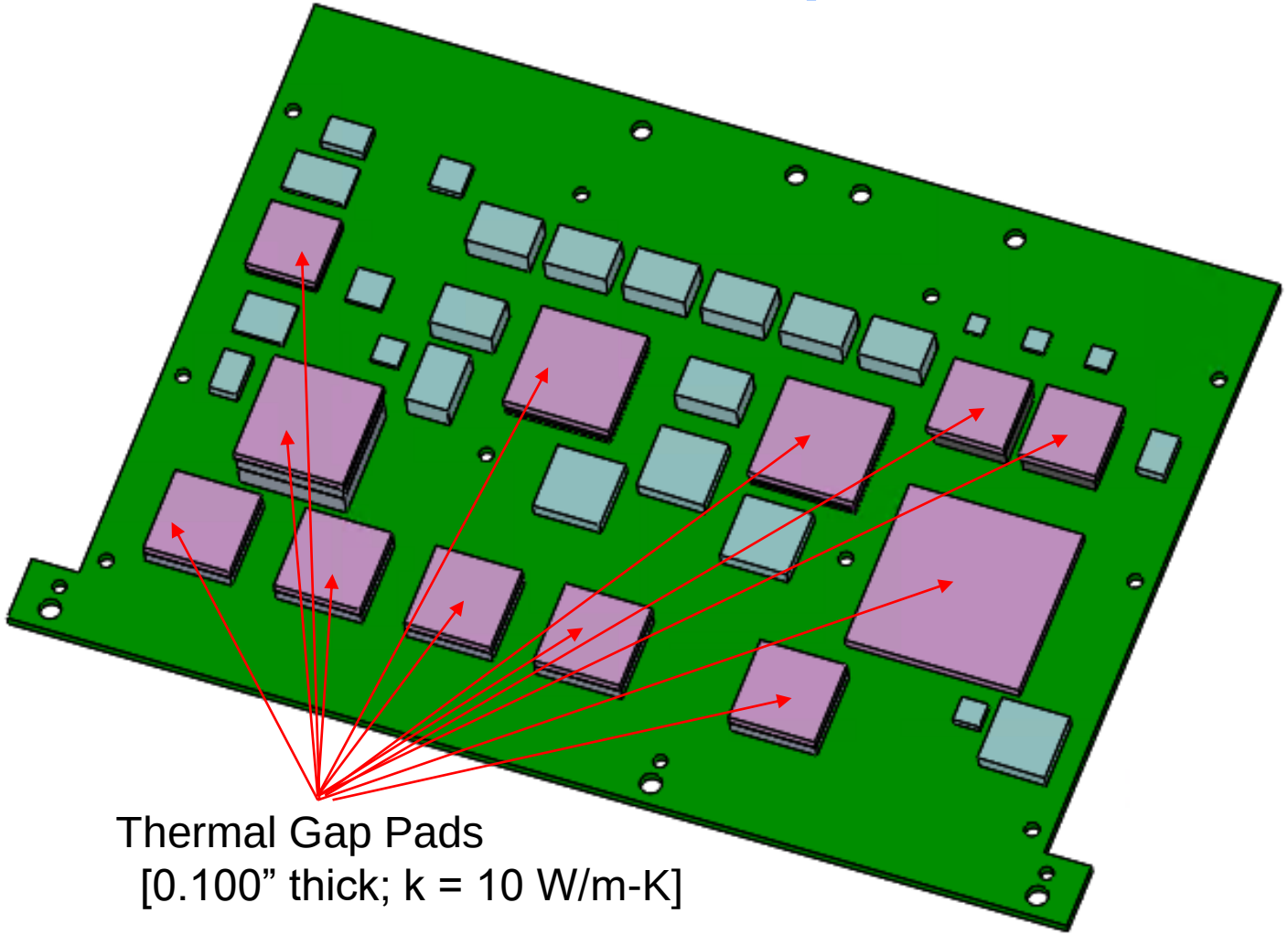
1. This analysis was done using FloTHERM XT V2019.3 CFD software.
2. The model was evaluated with solid conduction only with a fixed temperature applied to the cooling surface.
3. The thermal model was created from the cf-020400-01xm_asm.stp simplified for thermal analysis.
4. The boards were modeled based on the ODB++ files and initial estimates of the board.
5. It was assumed that no neighboring devices were producing or sinking heat.
6. The thermal gap pads on the components coupled to the front frame have a thermal conductivity of 10 W/m-K and are 0.100” thick.
7. The critical components were modeled as 2-resistor networks with thermal resistance values found on the “Parts Thermal Characteristics.doc”. All other non-critical components were assigned a lumped thermal conductivity of 5 W/m-K.
8. Metal-to-metal contact resistance was set to 0.298 C-in^2/W (equivalent to 5 micron air gap).
9. Note that it is assumed that the cover does not make direct contact with the PCBA.

Thermal Model Setup

Thermal Model Setup –Overview: PCB

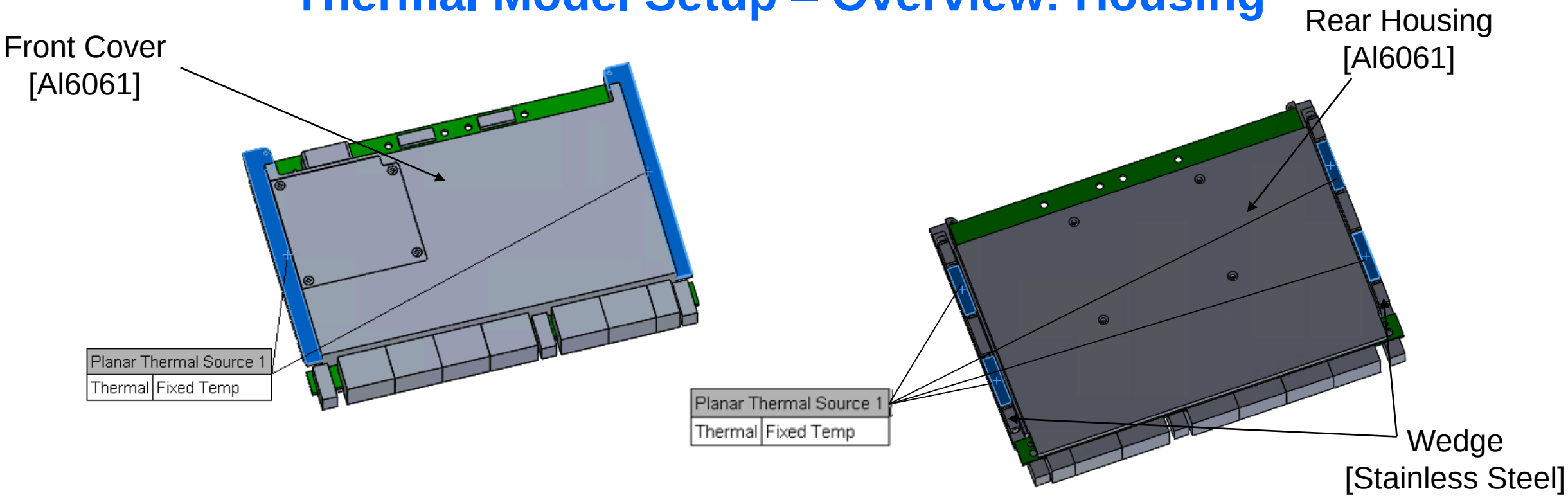


Thermal Model Setup – Overview
Board Thermal Gap Pads



Thermal Gap Pads
[0.100” thick; k = 10 W/m-K]

Thermal Model Setup – Overview: Housing



Note: The cooling surface contacts are shown in blue. The contact surface temperature is fixed in the thermal simulation. The value is chosen as the operating ambient temperature.

Screws (in frame assembly): [300 Series Stainless Steel]

Thermal Data

CF-0220011-01X	SNC Op. (W)			10G Op. (W)			Worst Case (W)			Thermal Resistance (ºC/W) / Model		Maximum Temperature (ºC)
Component	Qty	Per Component	Total	Qty	Per Component	Total	Qty	Per Component	Total	R_{JC}	R_{JB}	
CPU	1	4.67	4.67	1	4.67	4.67	1	7.8	7.8	2.57	6.89	115 (junction)
LTM4650 (0.88/1V)	1	2.1	2.1	1	2.32	2.32	1	4.3	4.3	3.7	1.5	125 (junction)
LTM4650 (1V Core)	1	1.17	1.17	1	1.52	1.52	1	1.74	1.74	3.7	1.5	125 (junction)
Aldrin	1	21.02	21.02	1	23.18	23.18	1	43	43	0.16	1.72	110 (junction)
TLK [U35A]	1	3.3	3.3	1	3.3	3.3	1	18.5	3.7	0.2	7.9	105 (junction)
TLK [U35B]	1	3.3	3.3	1	3.3	3.3	1	18.5	3.7	0.2	7.9	105 (junction)
TLK [U35C]	1	3.3	3.3	1	3.3	3.3	1	18.5	3.7	0.2	7.9	105 (junction)
TLK [U35D]	1	3.3	3.3	1	3.3	3.3	1	18.5	3.7	0.2	7.9	105 (junction)
TLK [U35E]	1	3.3	3.3	1	3.3	3.3	1	18.5	3.7	0.2	7.9	105 (junction)
Transceiver	1	4.29	4.29	1	4.29	4.29	1	6	6	Lumped Model k=113 W/m-K		85 (case)
Quad PHY [U37A]	1	13.12	13.12	1	13.12	13.12	1	13.5	13.5	0.3	2.6	105 (junction)
Quad PHY [U37B]	1	6.52	6.52	1	13.12	13.12	1	13.5	13.5	0.3	2.6	105 (junction)
PCB (Misc. spread)	1	5.33	5.33	1	5.90	5.9	1	122.86	7.26			
		Total	**74.72**		**Total**	**84.62**		**Total**	**115.6**			

Note: Thermal resistances from junction to case (R_{JC}) and from junction to board (R_{JB}) and thermal limits were taken from “Parts Thermal Characteristics”.

Thermal Analysis

ElectronicCooling Solutions inc

Results Summary

Power Scenario				SNC Op.			10G Op.			Worst-case		
Parameters												
TIM Thermal Conductivity, W/m-K					10			10			10	
Ambient Temp., °C					70			70			70	
Fixed Temp. on Cooling Surface, °C					70			70			70	
Elevation, ft					0			0			0	
RESULTS												
Component	Min. Limit, °C	Max. Limit, °C	Limit Type	Power, W	Result, °C	Margin, °C	Power, W	Result, °C	Margin, °C	Power, W	Result, °C	Margin, °C
CPU	-40	115	junction	4.67	89.2	25.8	4.67	89.8	25.2	7.8	101	14.0
LTM4650 (0.88/1V)	-40	125	junction	2.1	88.9	36.1	2.32	92.0	33.0	4.3	103	22.0
LTM4650 (1V Core)	-40	125	junction	1.17	85.1	39.9	1.52	88.1	36.9	1.74	94.3	30.7
Aldrin	-40	110	junction	21.02	91.6	18.4	23.18	94.5	15.5	43	110	0.0
TLK [U35A]	-40	105	junction	3.3	85.8	19.2	3.3	87.7	17.3	18.5	93.1	11.9
TLK [U35B]	-40	105	junction	3.3	87.8	17.2	3.3	89.7	15.3	18.5	94.8	10.2
TLK [U35C]	-40	105	junction	3.3	87.4	17.6	3.3	89.0	16.0	18.5	93.5	11.5
TLK [U35D]	-40	105	junction	3.3	85.0	20.0	3.3	86.2	18.8	18.5	89.9	15.1
TLK [U35E]	-40	105	junction	3.3	80.1	24.9	3.3	80.7	24.3	18.5	83.1	21.9
Transceiver	-40	85	case	4.29	82.5	2.5	4.29	83.6	1.4	6	87.3	-2.3
Quad PHY [U37A]	-40	105	junction	13.12	96.1	8.9	13.12	98.1	6.9	13.5	103	2.0
Quad PHY [U37B]	-40	105	junction	6.52	89.4	15.6	13.12	97.4	7.6	13.5	103	2.0

With the cooling plate at 70°C, all components remain below their maximum temperature rating for the SNC and 10G scenarios.

Note that the Transceiver overheats for the worst-case power dissipation scenario; the temperature is 2°C higher than the maximum limit for worst case.

Results Summary (Continued)

Power Scenario				SNC Op.			10G Op.			Worst-case		
Parameters												
TIM Thermal Conductivity, W/m-K					10			10			10	
Ambient Temp., °C					-10			-10			-10	
Fixed Temp. on Cooling Surface, °C					-10			-10			-10	
Elevation, ft					0			0			0	
RESULTS												
Component	Min. Limit, °C	Max. Limit, °C	Limit Type	Power, W	Result, °C	Margin, °C	Power, W	Result, °C	Margin, °C	Power, W	Result, °C	Margin, °C
CPU	-40	115	junction	4.67	9.6	49.6	4.67	10.1	50.1	7.8	21.3	50.1
LTM4650 (0.88/1V)	-40	125	junction	2.1	9.6	49.6	2.32	12.7	52.7	4.3	24	52.7
LTM4650 (1V Core)	-40	125	junction	1.17	5.6	45.6	1.52	8.7	48.7	1.74	15.1	48.7
Aldrin	-40	110	junction	21.02	12.3	52.3	23.18	15.3	55.3	43	30.8	55.3
TLK [U35A]	-40	105	junction	3.3	6.6	46.6	3.3	8.5	48.5	18.5	14.3	48.5
TLK [U35B]	-40	105	junction	3.3	8.7	48.7	3.3	10.7	50.7	18.5	16	50.7
TLK [U35C]	-40	105	junction	3.3	8.2	48.2	3.3	9.9	49.9	18.5	14.7	49.9
TLK [U35D]	-40	105	junction	3.3	5.7	45.7	3.3	7.0	47.0	18.5	10.8	47.0
TLK [U35E]	-40	105	junction	3.3	0.6	40.6	3.3	1.3	41.3	18.5	3.68	41.3
Transceiver	-40	85	case	4.29	3.1	43.1	4.29	4.3	44.3	6	8.19	44.3
Quad PHY [U37A]	-40	105	junction	13.12	17.0	57.0	13.12	19.1	59.1	13.5	24	59.1
Quad PHY [U37B]	-40	105	junction	6.52	10.2	50.2	13.12	18.4	58.4	13.5	24.2	58.4

With the cooling plate at -10°C, all components remain well below their maximum temperature rating for all power dissipation scenarios.

Results Summary (Continued)

Power Scenario				SNC Op.			10G Op.			Worst-case		
Parameters												
TIM Thermal Conductivity, W/m-K					10			10			10	
Ambient Temp., °C					85			85			85	
Fixed Temp. on Cooling Surface, °C					85			85			85	
Elevation, ft					0			0			0	
RESULTS												
Component	**Min. Limit, °C**	**Max. Limit, °C**	**Limit Type**	**Power, W**	**Result, °C**	**Margin, °C**	**Power, W**	**Result, °C**	**Margin, °C**	**Power, W**	**Result, °C**	**Margin, °C**
CPU	-40	115	junction	4.67	104.0	11.0	4.67	105.0	10.0	7.8	116	-1.0
LTM4650 (0.88/1V)	-40	125	junction	2.1	104.0	21.0	2.32	107.0	18.0	4.3	118	7.0
LTM4650 (1V Core)	-40	125	junction	1.17	100.0	25.0	1.52	103.0	22.0	1.74	109	16.0
Aldrin	-40	110	junction	21.02	107.0	3.0	23.18	109.0	1.0	43	125	**-15.0**
TLK [U35A]	-40	105	junction	3.3	101.0	4.0	3.3	103.0	2.0	18.5	108	-3.0
TLK [U35B]	-40	105	junction	3.3	103.0	2.0	3.3	105.0	0.0	18.5	110	**-5.0**
TLK [U35C]	-40	105	junction	3.3	102.0	3.0	3.3	104.0	1.0	18.5	108	**-3.0**
TLK [U35D]	-40	105	junction	3.3	99.9	5.1	3.3	101.0	4.0	18.5	105	0.0
TLK [U35E]	-40	105	junction	3.3	95.0	10.0	3.3	95.7	9.3	18.5	98	7.0
Transceiver	-40	85	case	4.29	97.4	**-12.4**	4.29	98.5	**-13.5**	6	102	**-17.0**
Quad PHY [U37A]	-40	105	junction	13.12	111.0	**-6.0**	13.12	113.0	**-8.0**	13.5	118	**-13.0**
Quad PHY [U37B]	-40	105	junction	6.52	104.0	1.0	13.12	112.0	**-7.0**	13.5	118	**-13.0**

With the cooling plate at 85°C, the Quad Phy (U37A) and the transceiver exceed their maximum temperature limits for each of the power dissipation scenarios.

Note that the maximum temperature rating for the transceiver is 85°C (same as the cooling plate temperature). The transceiver temperature will thus always be above 85°C.

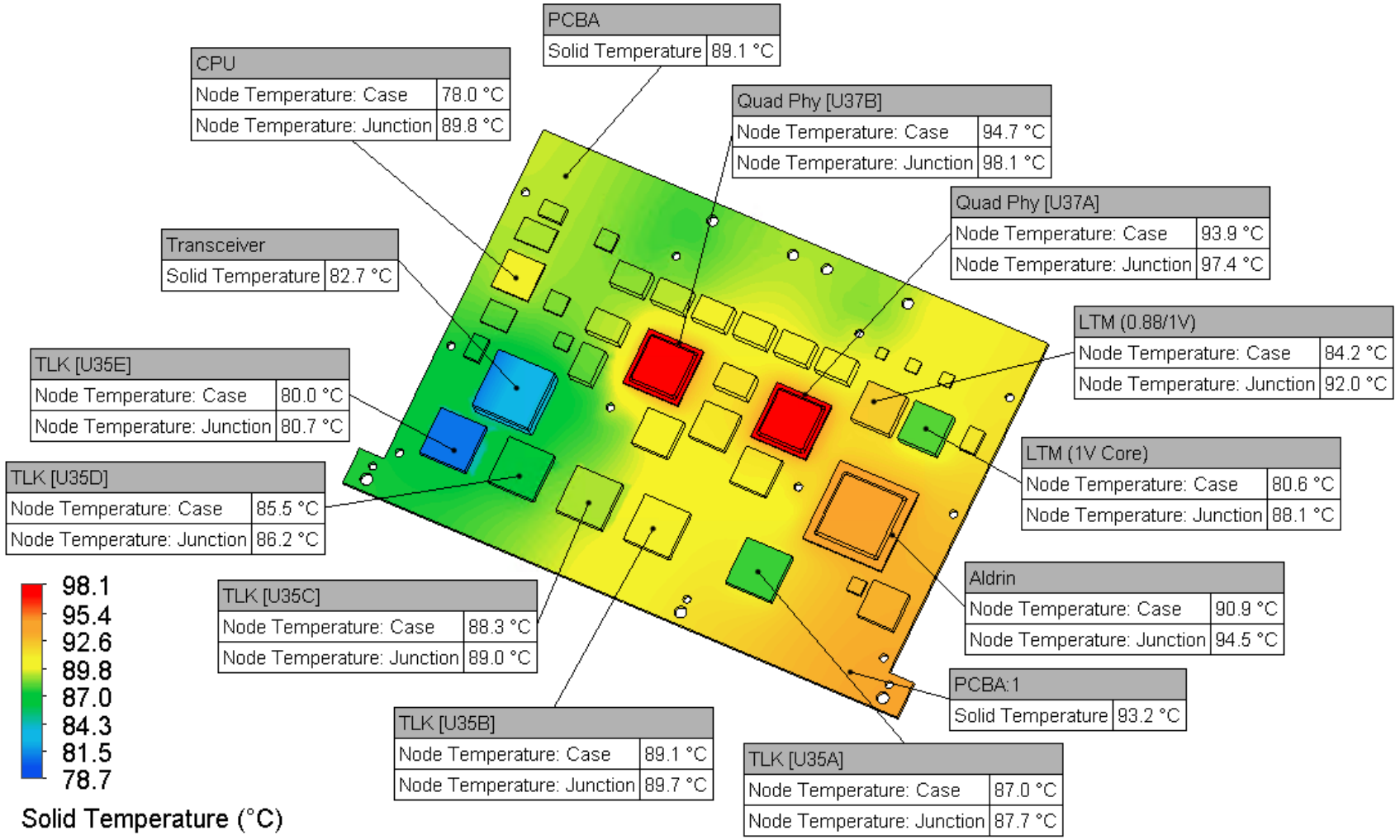
Results Summary (Continued)

Power Scenario				SNC Op.			10G Op.			Worst-case		
Parameters												
TIM Thermal Conductivity, W/m-K					10			10			10	
Ambient Temp., °C					-40			-40			-40	
Fixed Temp. on Cooling Surface, °C					-40			-40			-40	
Elevation, ft					0			0			0	
RESULTS												
Component	Min. Limit, °C	Max. Limit, °C	Limit Type	Power, W	Result, °C	Margin, °C	Power, W	Result, °C	Margin, °C	Power, W	Result, °C	Margin, °C
CPU	-40	115	junction	4.67	-20.1	19.9	4.67	-19.5	20.5	7.8	-8.24	31.8
LTM4650 (0.88/1V)	-40	125	junction	2.1	-19.9	20.1	2.32	-16.6	23.4	4.3	-5.1	34.9
LTM4650 (1V Core)	-40	125	junction	1.17	-23.9	16.1	1.52	-20.7	19.3	1.74	-14.1	25.9
Aldrin	-40	110	junction	21.02	-17.1	22.9	23.18	-14.0	26.0	43	1.84	41.8
TLK [U35A]	-40	105	junction	3.3	-22.7	17.3	3.3	-20.7	19.3	18.5	-14.7	25.3
TLK [U35B]	-40	105	junction	3.3	-20.5	19.5	3.3	-18.4	21.6	18.5	-13	27.0
TLK [U35C]	-40	105	junction	3.3	-21.0	19.0	3.3	-19.2	20.8	18.5	-14.3	25.7
TLK [U35D]	-40	105	junction	3.3	-23.6	16.4	3.3	-22.3	17.7	18.5	-18.3	21.7
TLK [U35E]	-40	105	junction	3.3	-29.0	11.0	3.3	-28.3	11.7	18.5	-25.7	14.3
Transceiver	-40	85	case	4.29	-26.3	13.7	4.29	-25.1	14.9	6	-21	19.0
Quad PHY [U37A]	-40	105	junction	13.12	-12.2	27.8	13.12	-10.0	30.0	13.5	-4.89	35.1
Quad PHY [U37B]	-40	105	junction	6.52	-19.0	21.0	13.12	-10.7	29.3	13.5	-4.7	35.3

With the cooling plate at -40°C, all components remain well below their maximum temperature rating for all power dissipation scenarios.

Board Surface Temperature Plot

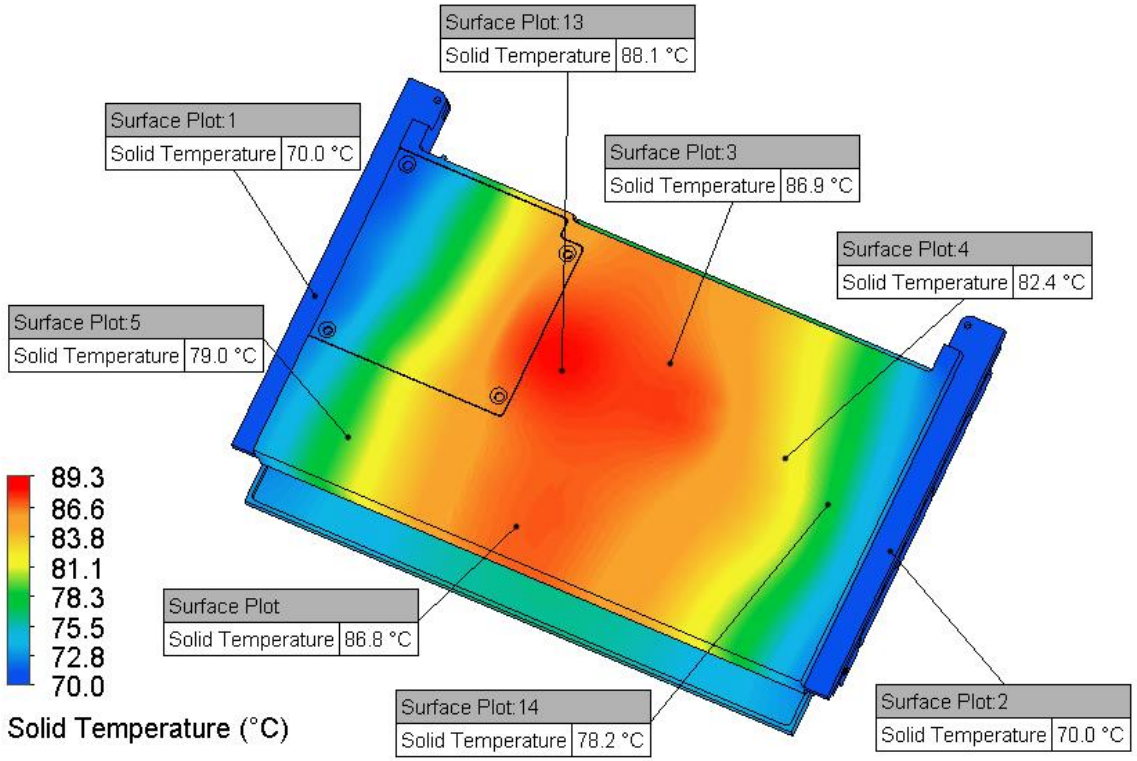
10G Op., 70°C , sea level

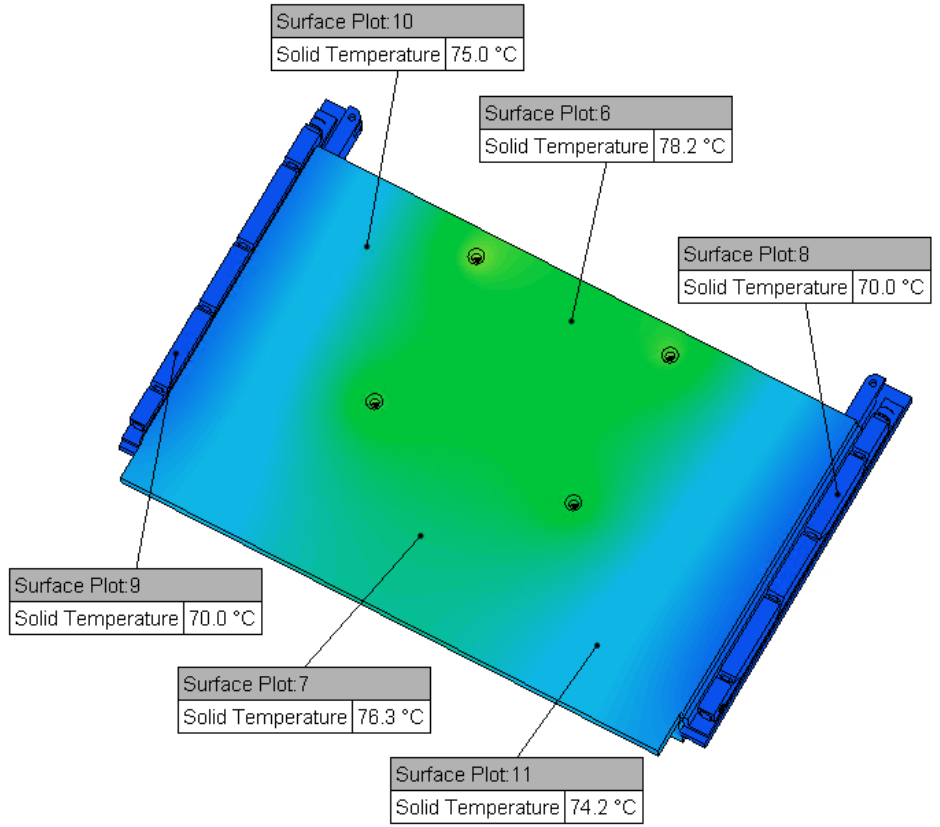


Note: Surface plot is showing internal or junction temperatures for 2-Resistor network components. Case temperature values are shown since this is the limit type specified for transceiver.

Housing Surface Temperature Plot

10G Op., 70°C , sea level



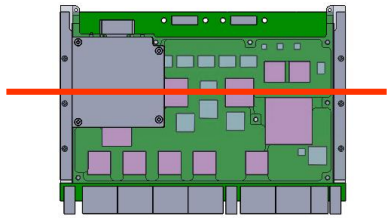


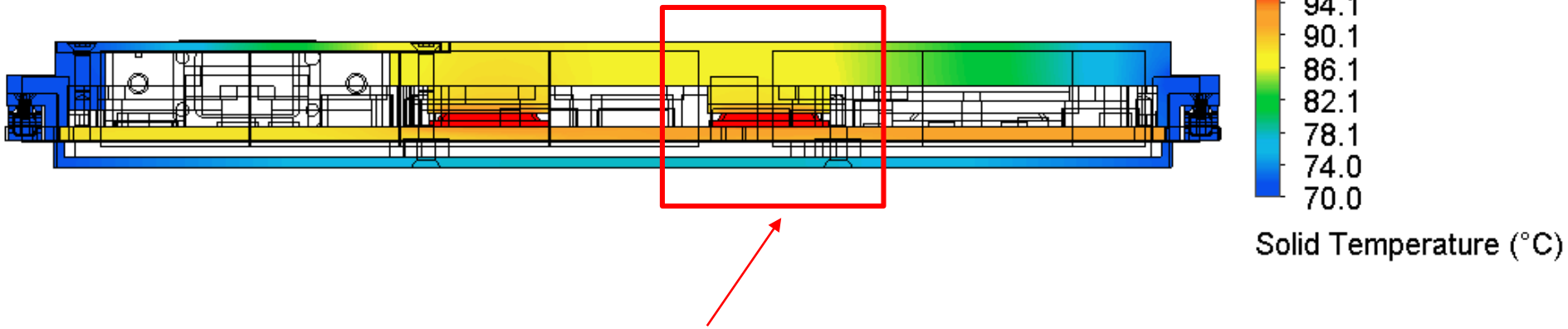
- There is a 18°C temperature gradient on the external surface of the front housing.
- There is about 8°C temperature gradient between the wedge and the rear cover.

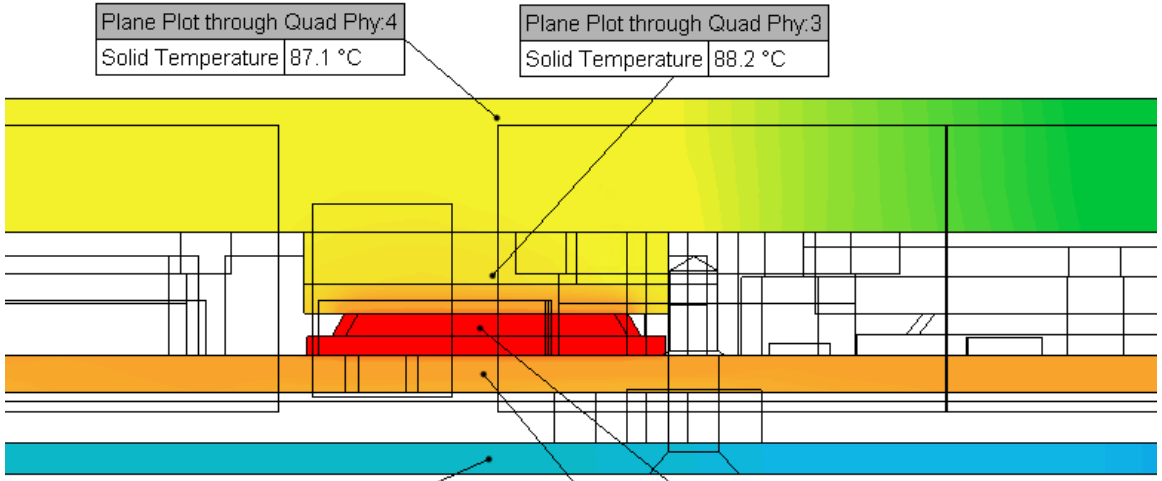
Cutplane Temperature Plot: Quad PHY

10G Op., 70°C , sea level

CUTPLANE LOCATION:





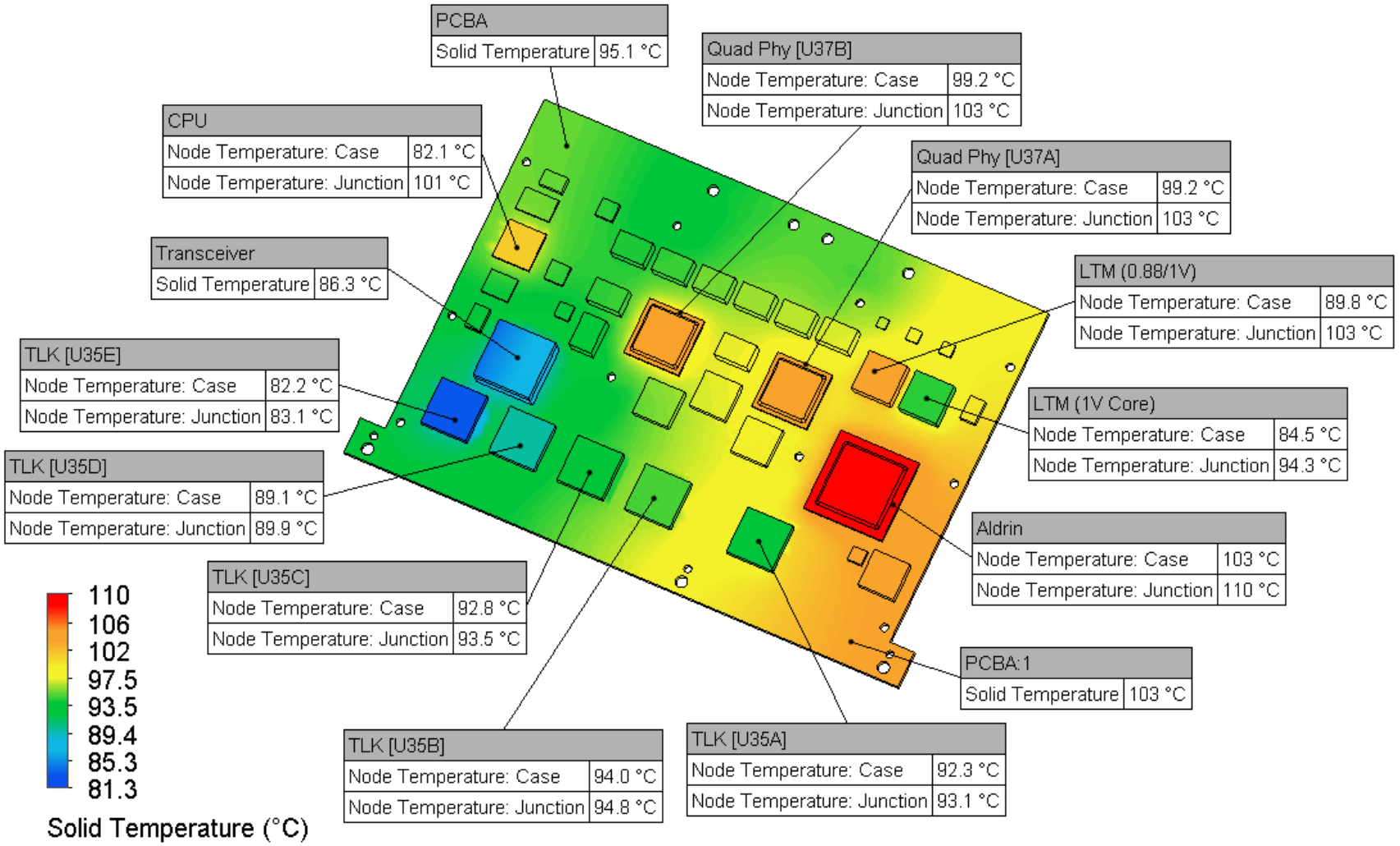


Note that the temperature gradient across the PCB and the rear cover is about 14°C.

Also note that the gradient across the thermal gap pad installed on the Quad Phy is 6°C.

Board Surface Temperature Plot

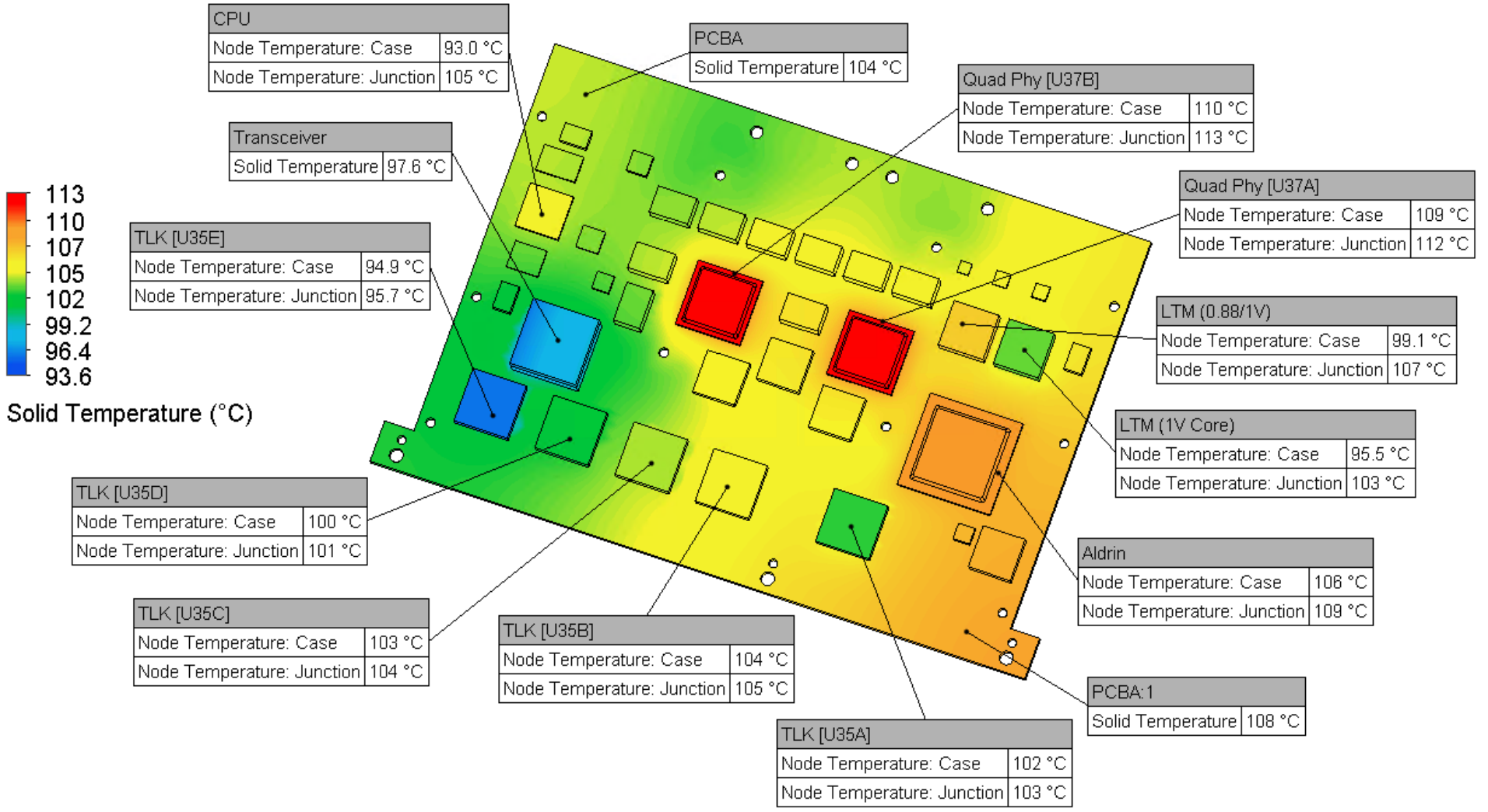
Worst Case., 70°C , sea level



Note: Surface plot is showing internal or junction temperatures for 2-Resistor network components. Case temperature values are shown since this is the limit type specified for transceiver.

Board Surface Temperature Plot

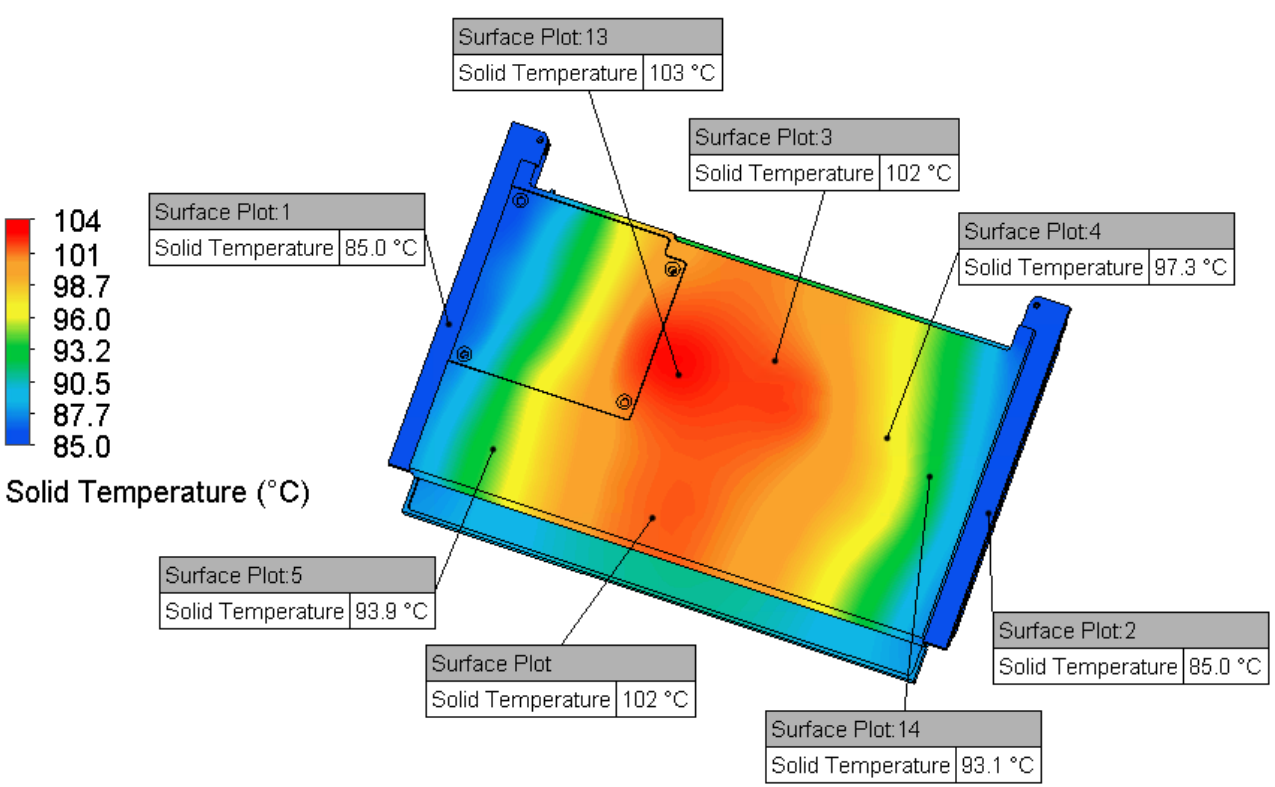
10G Op., 85°C , sea level

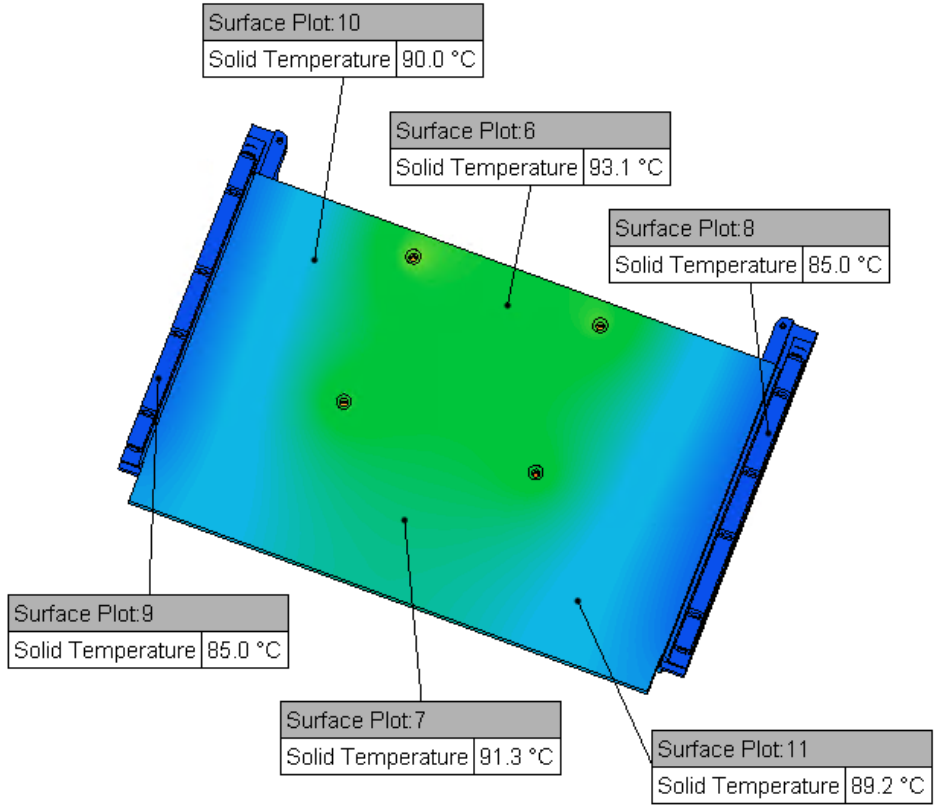


Note: Surface plot is showing internal or junction temperatures for 2-Resistor network components. Case temperature values are shown since this is the limit type specified for transceiver.

Housing Surface Temperature Plot

10G Op., 85°C , sea level



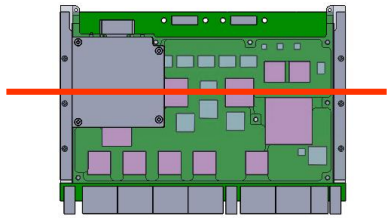


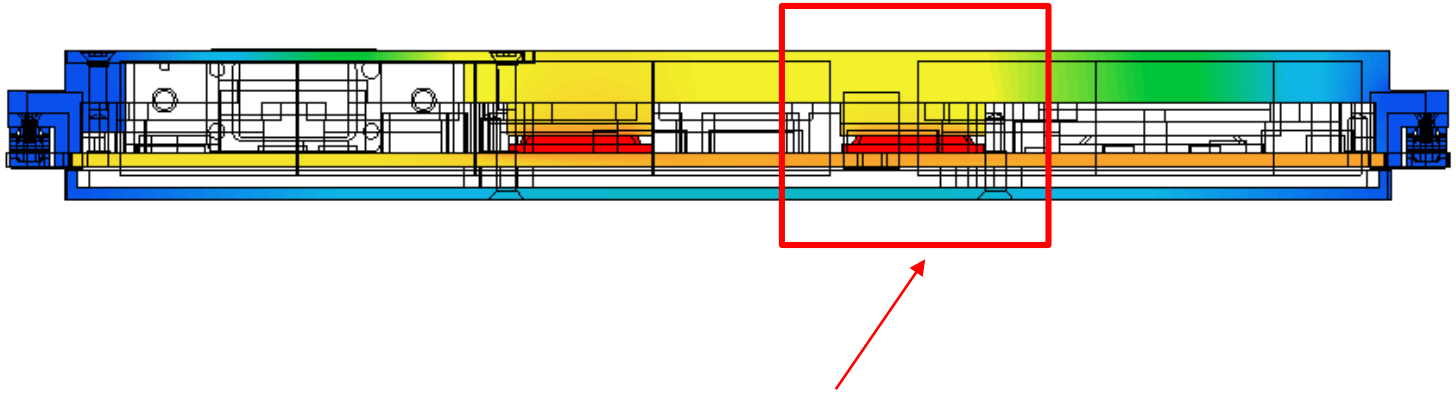
- There is a 18°C temperature gradient on the external surface of the front housing.
- There is about 7°C temperature gradient between the wedge and the rear cover.

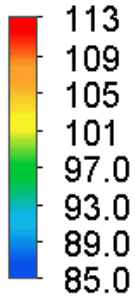
Cutplane Temperature Plot: Quad PHY

10G Op., 85°C , sea level

CUTPLANE LOCATION:

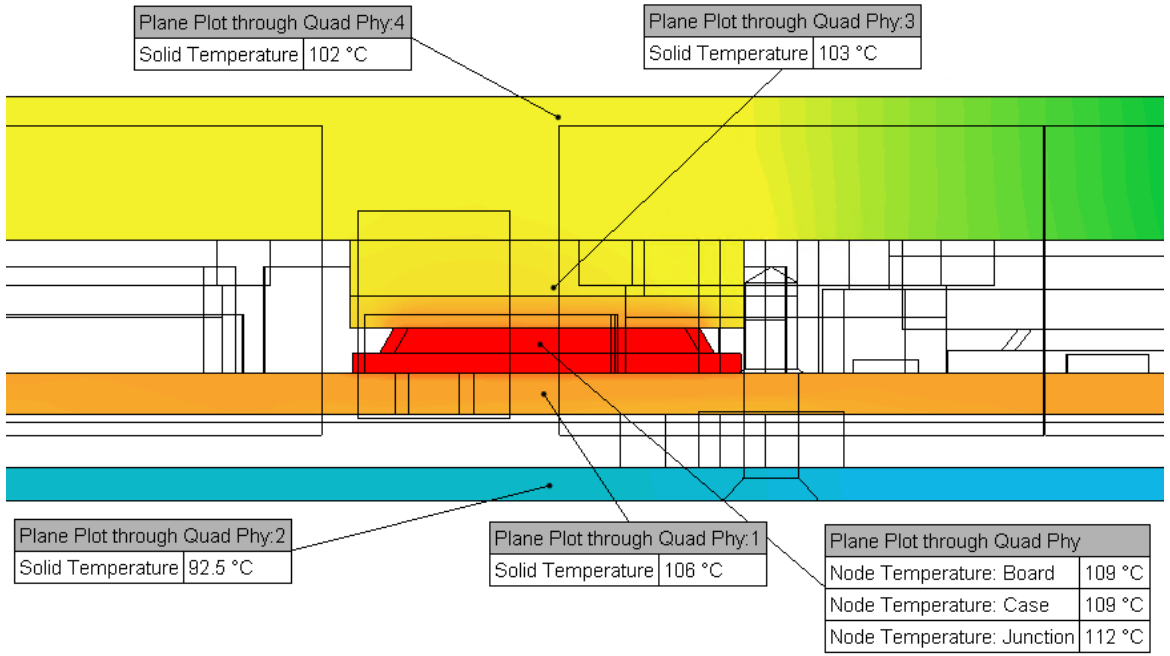






Note that the temperature gradient across the PCB and the rear cover is about 14°C.

Also note that the gradient across the thermal gap pad installed on the Quad Phy is 6°C.



Recommendations

- Below is the table of recommended cooling surface/cold plate temperatures based on the current configurations:

	Operating Mode		
Operating Mode	**SNC Op.**	**10G Op.**	**Worst-Case**
Minimum Cooling Plate Temperature* [°C]	-40	-40	-40
Maximum Cooling Plate Temperature [°C]	+73	+71	+68

* lower temperatures can be supported from a cooling standpoint. It is suggested to look into the minimum operating temperatures for the components.

- Notes:
  - ⇒ For the worst-case power scenario at 70°C cold plate temperature, the transceiver exceeds the maximum temperature limit by the largest negative margin. Therefore the transceiver dictates the required cooling surface temperature.
  - ⇒ For the 85°C cold plate temperature and for all corresponding power scenarios, the transceiver temperature determines the required cooling surface temperature.
  - ⇒ As longs as the cold plate surface temperature stays below the maximum value in the last row, all components operate within their thermal limits.